Driving Fully-Adiabatic Logic Circuits Using Custom High-*Q* MEMS Resonators

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Abstract

To perform digital logic in CMOS in a truly adiabatic (asymptotically thermodynamically reversible) fashion requires that logic transitions be driven by a quasi-trapezoidal (flat-topped) power-clock voltage waveform, which must be generated by a resonant element with a very high Q (quality factor). Recently, MEMS resonators have attained very high frequencies and Q factors, and are becoming widely used in communications SoCs for RF signal filtering, amplification, etc. In the ADIAMEMS project at the University of Florida, we are designing custom MEMS resonators for driving fully-adiabatic pipelined logic based on the 2LAL (two-level adiabatic logic) family previously developed at UF. The resonator design is being optimized to maximize its effective Q factor and area efficiency, at a frequency chosen to maximize the power-performance advantage of the adiabatic logic. Our analyses indicate that the adiabatic approach will eventually lead to orders-of-magnitude improvements in power-performance and even cost-performance, compared to competing approaches, for all power-limited applications. As competitive pressures drive down device costs, power dissipation will increasingly become the limiting factor on performance for most computing applications, and the advantages of the adiabatic approach will become ever greater.

Keywords: Adiabatic circuits, MEMS, low-power design, resonators, ultra-low-power.

1. Introduction

The concept of *adiabatic* (or thermodynamically reversible) digital transistor-based circuits has been around since at least the 1970s, when it was studied by Ed Fredkin and Tomasso Toffoli in the Information Mechanics group at MIT [1]; a mostly-adiabatic logic was even proposed by Boyd Watkins at Philco-Ford as early as 1967 [2]. During the 80's and 90's, advances in the understanding of reversible circuit concepts at MIT [3], Caltech [4], and ISI [5] led to the development of the first fully-adiabatic sequential logic styles (CRL and SCRL) by Younis and Knight at MIT [6,7], and to a small storm of literature on adiabatic circuits in the low-power design community since then.

Unfortunately, many engineers who tried adiabatic design were unaware of some relevant issues in thermodynamics and reversible computing theory, and as a result, many (perhaps most) of the published designs for purportedly "adiabatic" logic families actually contain design flaws that cause them to *not* be truly adiabatic, and that significantly limit the improvement in energy efficiency they can obtain.

Last year at MLPD '03, one of us (Frank) discussed the most commonly seen problems in published "adiabatic" designs, and how they can be avoided [8]. The most important rules that *must* be obeyed in order for a design to qualify as being truly adiabatic are (1) never pass current through a diode, (2) never turn on a transistor if there is a voltage across it ($V_{DS}\neq 0$), and (3) never turn *off* a transistor if there is a current through it ($I_{DS}\neq 0$). Together, these rules imply a requirement for reversible logic to be used (since logical information cannot be erased under these rules), and they also imply that logic gates must be driven by trapezoidal (not square-wave or sinusoidal) AC power-clock voltage waveforms.

Even when these rules are obeyed in the logic design, the driving signals must also be generated resonantly with very high *Q* (quality factor) if they are not to severely limit the gain in overall system energy efficiency that can be obtained by

using adiabatic logic. Unfortunately, waveform-generation circuits tend to have a low *Q* if they utilize either switching power MOSFETs [9] (to clamp the signal swing) or *LC* filter ladder-networks with integrated inductors. Transmission lines with customized impedance profiles have also been considered [10], but these have a less than ideal scaling of *Q* with frequency. Basically, all previous designs for the energy-recovering power supply are either low-*Q*, or require off-chip components that introduce significant additional parasitics.

In the SRC-funded ADIAMEMS (short for "Adiabatic MEMS") project at the University of Florida, we are exploring a novel solution for the power supply problem for adiabatic circuits, using custom resonators fabricated using MEMS (Microelectromechanical Systems) technology in an integrated CMOS/MEMS process. MEMS technology was selected since resonators with very high quality factors (above 10,000) as well as ones very high frequency (up into the GHz range) have been demonstrated [11]. MEMS resonators are being used as low power micro-components in analog circuits for RF filtering, amplification, *etc.* in communications Systems-on-a-Chip (SoCs). Several fabrication processes already exist that can produce MEMS elements integrated with CMOS electronics on the same chip [12,13]. Finally, the sinusoidal waveform normally produced by an oscillating MEMS structure can be remapped to a trapezoidal format by tailoring the shape-profile of the structures (*e.g.*, comb fingers) used for electromechanical transduction. High *Q* can be achieved by reducing gas and structure damping using vacuum packaging, advanced CMOS processes, and careful structural design.

Based on the early design and analysis work performed so far, we expect that our resonator designs may soon achieve an effective *Q* factor as high as 100 or more, using an area not much greater than that of the logic circuit being driven. We have taped out a prototype resonator design and will test it for driving a simple adiabatic logic circuit implemented in an available MOSIS process (probably TSMC 0.18 µm) and designed using the 2LAL (two-level adiabatic logic) design style, a simple fully-adiabatic logic family previously developed at UF [14]. We will measure total power dissipation using nanowatt-sensitive calorimetry techniques based on passive thermoelectrics [15]. We expect to show a significant (order of magnitude or greater) boost in power-performance compared to the best that can be achieved using traditional (non-adiabatic) voltage-scaled CMOS in the same process.

2. The 2LAL logic family

For purposes of this project, we are using a simple adiabatic logic design style called 2LAL (2-level adiabatic logic) developed at UF in Feb. 2000. As per its name, 2LAL uses two distinct voltage levels (high and low), like conventional CMOS, but unlike some earlier adiabatic logic styles such as SCRL (Split-Level Charge Recovery Logic). 2LAL, like SCRL, permits pipelined sequential circuits, while avoiding a bug that caused non-adiabatic dissipation in the original version of SCRL. 2LAL also has some very nice additional properties including:

1. **Short cycle time**: only 4 adiabatic transition times (4*t*) per complete clock period.
2. **Low latency**: only 1*t* (tick) of latency per logic level / pipeline stage.
3. **Low number of supply rails**: only 4 distinct driving signals need be supplied.

The first of these properties implies a low initiation interval (thus high throughput) for pipelines of 2LAL gates. Also, transitions take place over an entire ¼ of the clock cycle, the maximum possible in fully-adiabatic logic. This minimizes energy dissipation for transitions occurring at a given clock frequency. It also minimizes the slope of transitions, making it easier to obtain the desired slope in the resonant power supply (see next section), and it minimizes the duty cycle (active high time / cycle time), which makes it easier for the power supply to keep the high/low signal levels constant. A cycle time of 4*t* means a trapezoidal signal that is as close as possible in shape to a sine wave, and thus is easiest for a resonator to generate with high *Q*, since there's less energy in the higher-order harmonics.

The second property, of only 1 transition time *t* or "tick" of latency per logic level guarantees us the minimum possible time for information to propagate down a logic pipeline, given the transition time, and thus minimizes stalling for data-dependent operations.

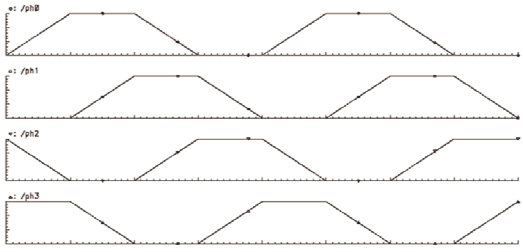

Figure 1. Clock/power supply rails for 2LAL. These consist of 4 trapezoidal voltage waveforms φ_0-φ_3, each with 50% duty cycle and 25% transition time, at relative phases of 0°, 90°, 180° and 270°.

The third property, low number of supply rails, minimizes the area required for implementing the resonators, since as few as possible of them are needed. We need at least 4 signals for fully-adiabatic logic. Figure 1 shows the rails needed for 2LAL. The basic elements of 2LAL logic circuits are described in Figure 2 below.

We are currently designing (in Cadence) these and other basic 2LAL cells, as well as higher-level blocks such as single-bit and multi-bit adders, multipliers, *etc.* We are also developing fully-adiabatic DRAM and SRAM cells, omitted here to save space. Our goal in all this is to build a complete suite of practical fully-adiabatic building blocks, suitable for constructing microprocessors, DSPs, and ASICs. A longer-term goal is to develop a VHDL-like textual hardware description language for adiabatic circuits, and develop related design tools specialized for adiabatic design, including circuit synthesis, simulation, and validation tools. These would facilitate the design of fully-adiabatic circuits, which is presently fairly cumbersome when we are confined to using traditional languages, design tools, and notations.

3. Resonator requirements

Although we feel 2LAL is significant in and of itself, as being one of the first and simplest (in many ways) *truly, fully* adiabatic sequential logic families, the most novel goal of our project is to design a MEMS resonator suitable for resonantly generating (with high *Q*) the 4-tick trapezoidal waveforms needed to drive 2LAL circuits. The basic concept of the resonator is to use an oscillating mechanical element (*e.g.*, a flexing beam), whose motions are coupled electrostatically (via interdigitated comb fingers, or parallel plates) to the load, forming a variable capacitor (with oscillating capacitance value) in series with the load. A static DC bias applied to the fingers cre-

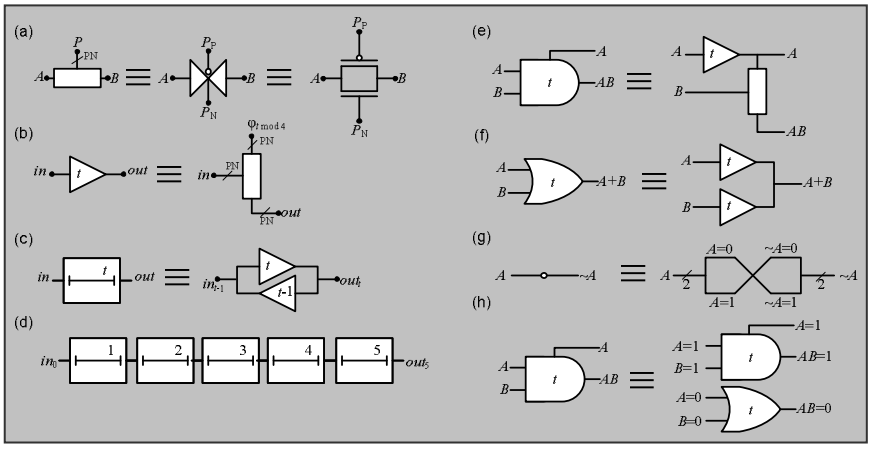

Figure 2. Basic 2LAL notation and gates. (a) Fundamental to 2LAL is the CMOS transmission gate, a parallel nFET/pFET pair whose control signal *P* is implicitly always a dual-rail pair of active-high (N) and active-low (P) logic signals. (b) A 4-transistor 2LAL buffer for dual-rail pulsed signals consists of two parallel transmission gates controlled by the input, passing a power-clock signal $\varphi_{t \bmod 4}$ and (implicitly in this drawing) its complementary, 180°-out-of-phase signal $\varphi_{(t+2) \bmod 4}$. The semantics is that if *in* pulses before tick #*t*, *out* will pulse @*t* (at tick #*t*), else it will stay at its initial level (arranged to be F). (c) An 8-transistor adiabatic delay element that moves an input pulse @*t*−1 to an output pulse @*t*. (d) Delay elements with subsequent tick numbers can be chained to make a shift register for input pulses. (e) An AND gate for pulses (8 transistors) consists of two transmission gates in series, and its internal node must be explicitly recognized as an extra output to maintain reversibility. (f) An 8-transistor OR gate for pulses consists of simultaneous transmission gates in parallel. (g) a zero-delay, zero-transistor, non-amplifying NOT bubble is implemented using quad-rail signaling; logic signal *A* is implemented as a pair of pulse signals, *A*=0 and *A*=1. A simple renaming of wires suffices to translate *A*=0 to ~*A*=1 and *A*=1 to ~*A*=0. (h) When fed a quad-rail input signal, an AND gate icon denotes a 16-transistor parallel pair of an AND and an OR (to compute *AB*=0 pulse). For all the logic gates, inputs may be consumed, if desired, by adding @*t*−1 reverse buffer elements, like in the delay element c.

ates a voltage divider, and an oscillating voltage level seen by the load. By custom-tailoring the detailed shape of the transducer structure (comb fingers), we can tune the position-capacitance response curve, and thus the voltage waveform shape, to match (in theory) any desired periodic and time-reversal symmetric function, such as the trapezoidal waveform we require. A small AC drive signal at the resonant frequency pumps up the oscillation amplitude and continuously replenishes the energy that is dissipated in the resonator and in the adiabatic transitions.

Important figures of merit (quantities to maximize) in the resonator design include:

1. **Effective quality factor** for transitions $Q_{\text{eff}} = E_{\text{tr}}/E_{\text{diss}}$, where E_{tr} is the energy transferred to or from the load on each transition, and E_{diss} is the energy dissipated in the resonator per clock cycle.
2. **Area-efficiency** $\alpha_{\text{E}} = A/E_{\text{tr}}$, where A is the resonator area and E_{tr} is the energy transferred. This determines the ratio between the area consumed by the resonator and that consumed by the logic, which affects the cost overhead of the adiabatic solution.

Important figures of demerit (quantities to minimize) in the resonator design include:

1. **Maximum transition slope** $s_{\max} = (\mathrm{d}C/\mathrm{d}t)_{\max} /(\Delta C_{\max}/\Delta t_{\text{tr}})$, where C is the instantaneous sense-structure capacitance, t is real time, $\Delta C_{\max}$ is the total capacitance swing needed to obtain the desired voltage variation, and $\Delta t_{\text{tr}} = 1/4f$ is the transition time, ¼ of the clock period in the case of 2LAL. Ideally the entire capacitance swing should occur at a constant rate, in which case $s_{\max}$=1, but a non-ideal waveform might have a steeper slope than this in some places. The $s_{\max}$ value lets us derive an upper bound on the total energy dissipation of the logic transition, as a multiple of that for the ideal ($s_{\max}$ = 1) case.
2. **Fractional capacitance variation** $v_C = \Delta C_{\text{var}}/\Delta C_{\max}$, where ΔC_{var} is the maximum range of sense-structure capacitance during the ¼ of a cycle during which the capacitance (and output voltage) is supposed to remain constant. This can be used to give us an upper bound on the maximum voltage mismatch ΔV that may occur whenever two circuit nodes are connected that are nominally supposed to be at equal logic levels; this mismatch leads to a $\frac{1}{2}C(\Delta V)^2$ dissipation that would not occur in the ideal case.

Finally, the resonant frequency f of the resonator structure should not itself necessarily be minimized or maximized, but rather should be chosen so as to maximize the overall power-performance (or cost-performance) of the overall design, that is, the resonator together with the logic.

4. Resonator design

The resonator design is illustrated in Figure 3(a). It consists of microstructures for both actuation and sensing. Interdigitated comb drives are used for signal transduction, just as in most common electrostatic actuators. The uniqueness of this resonator design lies in the sensing structure. As shown in Figure 3(b), the sensing structure is composed of comb fingers with a wide portion at the end. This unusual comb finger geometry is used to create a non-sinusoidal waveform when the resonator oscillates sinusoidally. The shape profile was carefully tailored such that a quasi-trapezoidal waveform would be generated (see Figure 4). The resonator can be made of poly-silicon or single-crystal silicon depending on the available microfabrication technology.

During operation, a DC bias voltage V_b is applied to the movable comb fingers of both actuation and sensing structures, while another DC plus AC voltage signal ($V_c + v_{\text{ac}}$) is applied to the stationary comb fingers of the actuation structure. The equivalent circuit with the applied voltages and output is shown in Figure 3(c), where C_{a}, C_{s} and C_{l} are respectively the actuator, sense and load capacitances.

The electrostatic force generated by the actuation comb fingers is given by

$$F_{\text{e}} = \frac{1}{2}\frac{\partial C_{\text{a}}}{\partial x}\left(V_{\text{p}} + V_{\text{ac}}\cos\omega t\right)^2$$
$$= \frac{1}{2}\frac{\partial C_{\text{a}}}{\partial x}\left(V_{\text{p}}^2 + \frac{V_{\text{ac}}^2}{2} + 2V_{\text{p}}V_{\text{ac}}\cos\omega t + \frac{V_{\text{ac}}^2}{2}\cos 2\omega t\right),$$

where $V_{\text{p}} = V_{\text{c}} - V_{\text{b}}$. To suppress the second harmonic term, V_{p} is set much greater than V_{ac}. When operating at its resonant frequency, the vibration amplitude of the fundamental frequency term will be multiplied by a factor of Q and will be the dominant term for the force. The maximum applied voltage is limited by the oxide

breakdown and the air breakdown voltage. Since our resonator has a small air gap (~.1 µm), air breakdown will be the dominant voltage limiter. The air breakdown voltage is approximately 110 V per µm of air gap [16]. So, the maximum applied voltage is about 10V. Simulation shows that sufficient displacement can be achieved at V_p = 10V. The output voltage V_o can be much smaller than 10V, depending on the load capacitance, and will be tuned to the transistor operating voltage. Due to the high impedance output node, a buffer is used to drive the bonding pad for testing purposes.

CoventorWare [17], a finite-element simulation tool, was employed to design the sensing comb fingers to generate the desired output waveforms. One example waveform is shown in Figure 4. The flat top of the trapezoidal signal is realized by custom tuning the shape of the sense comb fingers as illustrated in Figure 3(b). The nearly flat bottom is due to the very small change of the fringing capacitance when the moving fingers are far from the stationary fingers. Note, as shown in Figure 3(a), when the resonator is at rest, the moving and stationary sensing comb fingers are separated by 3 µm. When the resonator moves to the maximum amplitude position, as shown in Figure 3(c), the minimum gap d_s between the sense comb fingers is as small as 0.1 µm. Gaps less than 0.1 µm are also achievable, but the maximum applied voltage will then be decreased due to air breakdown. Some design parameters are shown in Table 1. A 20 fF sense capacitance variation was achieved.

Note that the sensing capacitance variation is only ~0.2 fF per comb finger; however, it should be feasible to increase the structure thickness by a factor of 20 using a DRIE process to yield a figure closer to 4 fF per comb finger [13]. Using a bias voltage of 10 V, this means each comb finger could drive a load equivalent to about 40 minimum sized devices of about 1 fF load capacitance each, through a voltage swing of ~1V. The area needed for this many devices is comparable to the area occupied by the comb finger.

Table 1. Some key parameters of a prototype resonator at 0.5 MHz resonant frequency.

Thickness:	2 µm	Bias voltage V_b:	10 V
Min. gap size:	0.1 µm	DC drive voltage $\|V_c - V_b\|$:	10 V
Min. feature size:	0.5 µm	AC drive voltage v_{ac}:	0.2 V
# of actuation fingers N_a:	20	Area A:	107 µm ×36 µm
# of sensing fingers N_s:	106	Capacitance variation:	20 fF
Quality factor Q:	5000 (est.)	Effective quality factor Q_{eff}:	46
Vibration amplitude X:	4 µm	Area efficiency α_E	3.23× 10^{-4} J/m^2

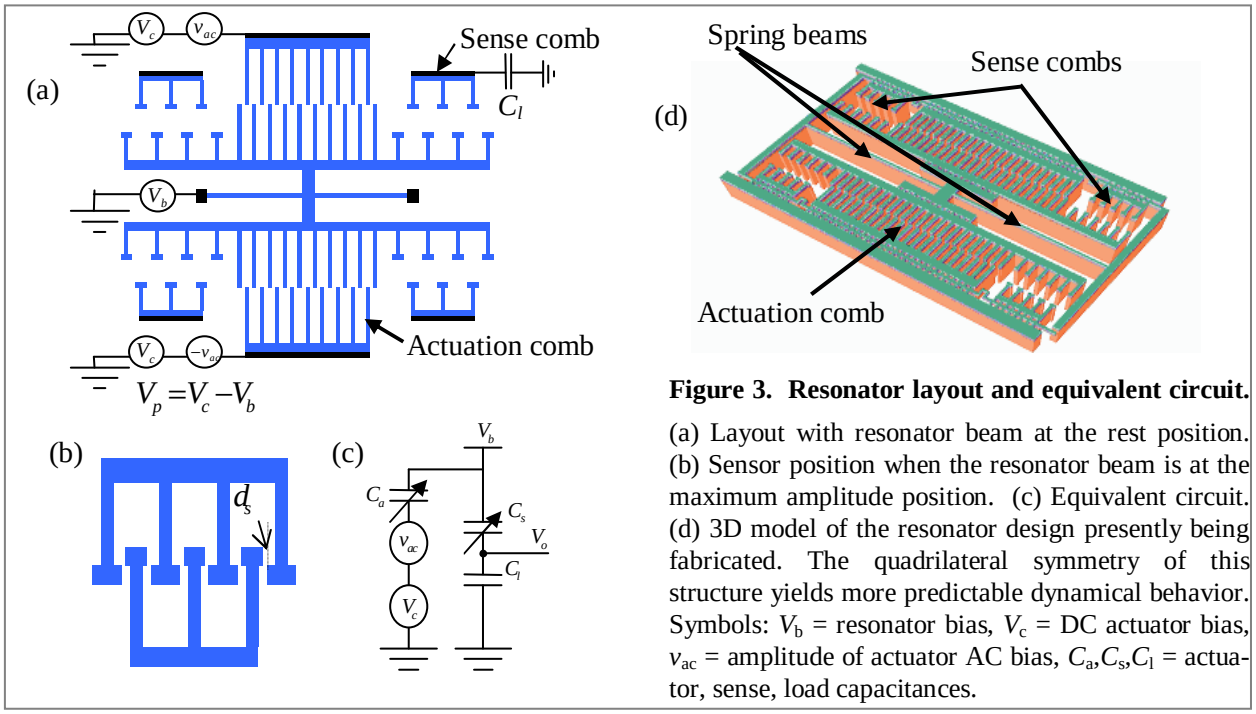

Figure 3. Resonator layout and equivalent circuit. (a) Layout with resonator beam at the rest position. (b) Sensor position when the resonator beam is at the maximum amplitude position. (c) Equivalent circuit. (d) 3D model of the resonator design presently being fabricated. The quadrilateral symmetry of this structure yields more predictable dynamical behavior. Symbols: V_b = resonator bias, V_c = DC actuator bias, v_{ac} = amplitude of actuator AC bias, C_a,C_s,C_l = actuator, sense, load capacitances.

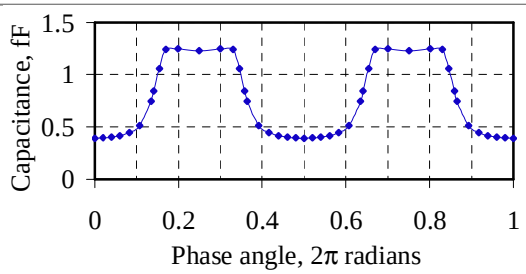

Figure 4. Simulated output waveform. Note the near-flat wave tops and bottoms. Additional refinement of the finger shape, together with additional compensating structures, is expected to further improve the wave shape to bring it even closer to the ideal trapezoidal waveform. Note the frequency doubling due to the symmetric structure.

5. Design optimization

To completely optimize the resonator design requires a joint system-level optimization in concert with the logic, in order to select the optimal operating frequency, voltages, and resonator area so as to maximize the overall gain in cost-performance from the adiabatic design. As of this writing, the complete analysis has not yet been done, since we are still exploring alternative resonator geometries. However, some aspects of the resonator design have already been optimized.

From the resonator point of view, given the limitation of air breakdown voltage, the optimization of Q_{eff} and α_E is done by ma ximizing the sense capacitance variation and minimizing the vibration amplitude and the resonator area. New regions of the design space need to be explored to further improve these parameters.

6. Projected results

As part of our work, we used simulations based on BSIM3 device models to calculate the maximum operating frequencies for logic in the TSMC 0.18 µm CMOS technology in which we are presently designing our 2LAL test circuits. Our preliminary results indicate that at an example ultra-low power level of ~7 pW per logic gate, ordinary voltage-scaled CMOS can run at a maximum frequency of only ~260 kHz, by operating in a subthreshold regime of V_{dd} = 240 mV, while adiabatic CMOS can run at up to ~12.7 MHz, at a much higher voltage of 1.65 V, while still satisfying the power constraint. The adiabatic performance boost is thus ~50× and the cost-efficiency boost is ~12 in ideal applications with only 4× adiabatic hardware overhead.

Although the peak frequency of ~13 MHz in this scenario is higher than achieved in our present resonator prototypes, further design refinements in a newer MEMS process should be able to move us into the MHz frequency range. Once this is done, based on our preliminary analyses, we expect to be able to empirically demonstrate roughly an order-of-magnitude reduction in energy dissipation in our MEMS/2LAL design compared with standard CMOS, when optimized using our design methodology. As MEMS technology pushes down towards the nanoscale, further refinements of these techniques are expected to lead to significant boosts in both performance and cost-performance for particularly power-limited applications in the near-term, and in the long term for the majority of high-performance computations.

7. Conclusion

The effectiveness of adiabatic techniques for low-power logic can be dramatically improved by using sound techniques in the circuit design, and high-quality components in the energy recovery system. MEMS technology appears to offer the right characteristics for the latter job. In the ADIAMEMS project at UF, we are taking the first steps towards demonstrating adiabatic techniques that could actually be commercially practical for ultra-low-power logic. A prototype MEMS resonator producing a high quality custom wave shape was successfully designed and sent out for fabrication. Meanwhile, test circuits are being constructed using the new 2LAL design style, and simulations indicate that a 50× performance boost might be achieved versus conventional CMOS in ultra-low-power application scenarios in a presently available process technology.

However, in the present project, we are really only getting "warmed up" for future applications of adiabatic technology. In the next few decades, as irreversible computing reaches its limits, and power becomes ever more dominant as a performance limiter, we expect that techniques such as those we have described will eventually dominate not only in the low-power market segment, but also in all high-performance computing [18], in-

cluding, for example, tightly-coupled supercomputing applications. In light of the immense future promise of adiabatics, we can confidently say: "You ain't seen nothin' yet."

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