DOCUMENT: **PROPOSAL ABSTRACT**

TITLE: **Practical Energy-Recycling Computation for Mobile Tactical Applications**

AGENCY: DARPA/ATO
PROGRAM: Advanced Technologies
BAA NUMBER: 00-27
PROGRAM POC: Dr. Parney Albright *fax*: 703-696-9781

TECHNICAL AREAS: **Early Entry/Special Forces/Light Forces:** Soldier self sustainability, personal communications, small/portable robotic devices. **Communications:** MEMS technology integration, advanced techniques to improve data throughput.

INSTITUTION: University of Florida, Departments of CISE and ECE
BUSINESS TYPE: OTHER EDUCATIONAL

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PERFORMANCE PERIOD: Year 1: 15 Aug 2000 - 14 Aug 2001 (12 months)
Year 2 option: 15 Aug 2001 - 14 Aug 2002 (12 months)
Year 3 option: 15 Aug 2002 - 14 Aug 2003 (12 months)
(Dates as per university guidelines; modifiable if sponsor requests.)

COST SUMMARY:

ESTIMATED YEAR-1 (BASE) COST:	$ 466,000
ESTIMATED YEAR-2 (OPTION) COST:	$ 447,000
ESTIMATED YEAR-3 (OPTION) COST:	$ 448,000
ESTIMATED TOTAL 3-YEAR PROJECT COST:	$1,361,000

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Four-page summary of Volume I Sections II,III,IV

Summary of II A. Innovative Claims

Motivation. In many systems of tactical importance, such as mobile communications systems, small robotic devices for surveilance or force delivery (e.g. autonomous submersibles), and many varieties of wearable or field-deployed electronic equipment, energy-efficient system operation is critical due to (1) the limited energy storage capacity of small, portable energy storage systems such as batteries and other chemical fuel systems, and (2) the difficulty of delivering replacement energy resources when needed into active battlefield environments.

Today, many of these tactical systems depend, to an increasing extent, on substantial amounts of electronic computing, for purposes such as signal processing, automated control, tactical displays, or situation analysis. In many systems, the electronics may indeed be the major component of the total system energy usage. It is therefore important to explore ways to reduce the energy required for computing as much as is possible.

Background. In the last decade, there have been significant advances in the field of so-called "adiabatic" digital electronics [1-10], a class of circuits which provides a means of reusing most of a system's active electrical energy from one computational cycle to the next, rather than dissipating all the energy on every cycle, as is done by all conventional circuits. In principle, the net energy consumption per operation can be made as small as desired, although in practice various technological factors conspire to limit the energy savings that can be achieved at reasonable levels of system cost. However, our research suggests that in small mobile applications where the effective cost of energy is relatively high (compared to fixed or large mobile installations), adiabatic techniques can potentially achieve significant benefits in overall cost-efficiency, compared to more conventional techniques.

Innovations. We have in mind several innovative ideas and directions in the adiabatic circuits arena that we would like to further develop in this research:

(1) We have ideas for new and more efficient techniques for designing adiabatic logic circuits and memory, which will require fewer transistors and input signals than earlier approaches.

(2) We would like to carry out accurate measurement of power characteristics of adiabatic circuits, and produce software models for automatic analysis and optimization of adiabatic system designs.

(3) We would like to explore the possible use of MEMS electrostatic mechanical switches or other low-resistance switching devices as a more energy-efficient alternative to transistor technology, for use in adiabatic power supplies and some logic circuits.

(4) We would like to produce an application-specific adiabatic demonstration system that shows a practical cost-efficiency benefit for a real energy-limited mobile application of interest to the DoD (we need help from DARPA, however, to learn more about the candidate applications and their requirements).

Summary of II B, III B: Deliverables, results, products, technology transfer.

We propose to produce the following results and deliverables, broken down by option year:

Year 1:

1) Detailed, precise experimental data on the power dissipation, performace and cost factors of fabricated adiabatic vs. conventional low-power circuits (including power supply).
2) Data and detailed analysis indicating whether MEMS switches or other advanced devices can be cost-effective for use in adiabatic circuits.
3) A complete design for a demonstration adiabatic power supply, amenable to further commercial or DoD development.

4) A complete mask-level design for an adiabatic logic chip that performs a signal-processing or other application function of practical use in tactical mobile systems, with lower minimum dissipation per operation than competing low-power solutions.
5) Design notes on item #4, to aid in the development of other adiabatic systems.
6) Working modeling software for comparing adiabatic vs. other low-power approaches to determine which approach has the greatest cost-efficiency given application constraints and requirements. Documentation included.

Optional year 2 extension:

7) Improved power supply design integrating MEMS or other advanced device technology if year 1 results indicate that is beneficial.
8) Improved design for application logic chip, incorporating lessons learned from metrology obtained in year 1 (item 1 above).
9) Complete integrated-system design (incorporating power supply and logic chip on a single circuit board or MCM) that is cost-effective in a practical application context.
10) Physical, fabricated sample parts for the design of #9, suitable for independent testing.
11) User's manual for the part in #10, including experimental power/performance data.
12) Improved version of modeling software from item #6.

Optional year 3 extension:

13) Detailed analysis extrapolating adiabatic design principles and cost-benefit tradeoffs to future technology environments: That is, comparison of cost-effectiveness with other competing emerging technologies, and consequent technology lifetime projections.
14) Additional refinements of year 2 items as requested by DoD.
15) Implementation of demonstration systems for additional applications.
16) In-depth technology transfer, working closely with DoD or industry contractors to usefully integrate the demonstrated technology into production systems.

Summary of II D, III C, III D: Technical rationale and technical approach.

Technical rationale.

Conventional digital computing circuits dissipate $CV^2/2$ energy per switching operation, where C is the capacitance of the circuit node in question, and V is the change in node voltage. However, in a non-standard switching process called *quasistatic*, *adiabatic*, or *reversible* charging, dissipation per operation can be reduced to approximately CV^2RC/t, where R is the switch resistance and $t >> RC$ is the amount of time taken to perform the switching action, as determined by an external clock signal. No digital information is lost in this kind of transition, so we say it is *logically reversible*. Theoretical computer scientists have long understood that any computation can be performed solely using logically reversible operations; but only in the last decade have detailed transistor-level designs been developed for fully-adiabatic, integrated, pipelined digital logic.

Although the CV^2RC/t formula seems to suggest that dissipation can be made arbitrarily small by increasing the transition time t, several factors conspire to limit the practical cost-effectiveness of this procedure. First is the obvious one that if the time t per operation is increased, then one must perform a corresponding larger number of simultaneous operations in parallel (using more digital hardware) to maintain the same overall throughput (number of operations per second), and further this is applicable only if the computation being performed is sufficiently parallelizable. (Fortunately, many important computations are indeed highly parallelizable.)

Despite this problem, there is a potential cost-effectiveness advantage for adiabatic technology in mobile computing situations where the effective cost $\$_E$ inherent in carrying along suf-

ficient energy resources for sustainability may exceed the cost $\$_{Si}$ of the required electronics itself. Consider, for example, the implicit costs resulting from of the reduction in effectiveness of a foot-soldier in a long-term field operation, if he is required to carry heavy battery packs for sustainability of his electronics systems, which may themselves be relatively lightweight.

For such situations, the adiabatic approach provides a new tradeoff opportunity, in which energy costs for a computation can scale as $\$_E/N$ (where N is the transition time increase factor), while silicon costs scale as $\$_{Si}N$, thereby permitting the mobile system designer to select the value of N that minimizes the total effective system cost $\$_E/N + \$_{Si}N$, thereby achieving greater overall mission cost-effectiveness. This energy-hardware tradeoff opportunity is not available in the traditional non-adiabatic approach, in which the energy cost for a computation cannot be reduced below the limit set by the $CV^2/2$ value.

A second limitation on the potential cost-effectiveness advantages of adiabatic systems results from difficulties in making the adiabatic clock-signal generators be as energy efficient as the logic itself. Many adiabatic power supply designs rely on irreversibly-driven switches, but if the switches used in the power supply are of no higher quality q (defined as conductance per unit of activation energy, $q = (1/R)CV^2$) than those in the logic circuit, then this turns out to limit the scaling of total system dissipation (including in the power supply) to only $t^{-1/2}$, rather than the ideal t^{-1} relation, which in turn decreases the maximum cost-efficiency benefits attainable in a given energy-limited application. (Though some benefit might still be attainable.)

One approach to minimizing this problem is to use a different switching technology in the power supply, one that provides higher-quality switches. Electrostatic MEMS switches are one class of candidates which seem to be capable of higher q than present-day MOSFET switches. However, research is needed to factor in the maximum frequency, reliability, and relative cost of MEMS switches into this analysis before we can confidently conclude that MEMS switching technology offers a clear cost-efficiency advantage in adiabatic systems. This research will be part of our project. We will also look for other potential ways to decrease switch resistance.

Another potential limiting factor is the resonant quality Q of the oscillatory elements which are used for energy storage in the adiabatic power supply. This Q directly limits the maximum energy savings factor achievable in the system. In addition to considering available inductor components, we also wish to study the possibility of using MEMS elements as resonant elements.

Finally, even if high-quality components are used in the power supply, there is a problem of leakage currents in the logic MOSFETs, which limits the maximum energy savings attainable. This particular factor is actually expected not to be the dominant energy bottleneck in present-day systems (limitations in the power supply will probably dominate instead), but as MOSFET technology progresses towards smaller feature sizes and lower voltages, leakage currents as a fraction of on-currents will increase rapidly, and eventually (at around 2010 by current projections) wipe out any potential energy savings from adiabatic techniques in those technologies.

However, in an energy-limited system, it is not necessarily best to use the technology with the smallest feature sizes. Rather, one may just stick with an earlier-generation technology where leakage is small. But if so, that imposes yet another silicon-area penalty on the low-power technology, when compared to high-performance technology using the smallest available feature sizes. In considering the long-term cost-effectiveness benefits achievable with adiabatic techniques, this is another factor that must be taken into analysis.

The overall aim of this research is to (1) accurately characterize the real, practical, cost-efficiency benefits that could be attained today using adiabatic electronics in energy-limited tactical applications, (2) build real demonstration systems that realize these benefits, (3) push the boundaries of the efficiencies that can be attained, by investigating novel device ideas such as MEMS technology, and (4) understand if and when the potential advantages of the adiabatic approach will be outweighed by continuing improvements in the mainstream line of computing technology.

Technical approach.

Our overall approach will be to build and test real systems. A purely theoretical approach would risk neglecting potential sources of energy dissipation. However, our work on design and experiment will be accompanied by theoretical analysis to guide the design work.

Measurements of total system energy dissipation (logic + resonant signal generator) can be done by simply integrating over time the instantaneous current flowing into the system from an external DC voltage source. We would also like to distinguish the dissipation in the clock generator from that in the logic. This is more difficult to do by just measuring currents because it would require picking out the relatively small net power dissipation remaining after cancellation of relatively large AC power transfers into and out of the logic circuit; this approach seems highly vulnerable to small measurement errors. Instead, we are planning to use calorimetry techniques to directly measure the heat output from the logic component, separately from the power supply. Peltier thermoelectric coolers have been used by an IBM group as sensitive thermocouples to measure extremely low power dissipation rates in adiabatic circuits [8]. We would like to replicate and improve on their technique.

To determine an appropriate target application, we would like to meet and talk with experts known to DARPA who are familiar with the requirements and characteristics of particular tactical computing systems; we are not yet ourselves intimately familar with detailed application needs in that arena. An introduction to an appropriate contact would be appreciated. Discussing the application needs with appropriate tactical systems experts would be a useful thing to do in an initial PI meeting.

To implement the chosen piece of application computing functionality in adiabatic circuits, we plan to use a variety of design techniques that were studied by Dr. Frank and his research colleagues during Ph.D. projects at MIT, augmented with some not-yet-published improvements that have been discovered more recently by Dr. Frank.

The adiabatic circuit will be compared against a convential circuit implementing the same functionality, as a control in experiments.

Our present analytical understanding of the cost-efficiency tradeoffs involved in the use of adiabatic circuits will be refined and embodied in a software model, together with academic articles and documentation explaining the analysis. The software will facilitate determining whether adiabatic circuits will be cost-effective in a particular application, and it will aid in optimizing parameters of the design.

MEMS technologies will be studied via collaboration with Dr. Nishida and other researchers, and will integrated into the cost-efficiency analysis to determine if they are viable in this context. If so, we will attempt to purchase access to a fabrication line (possibly a research facility at another institution) that is appropriate for building the MEMS systems we will need. We will also look at the possibility of MEMS and MOSFET integration onto the same die, but at the moment, we feel that separate dies are sufficient for our purposes.

Summary of IID, IIIA: Statement of Work, Constructive Plan

Each year's work is here broken down into "threads," along which work can proceed in parallel, partially independently of each other, but with interaction as needed. Different subsets of the team will be involved in different threads. Preliminary suggestions for team members primarily involved in each thread are given in parentheses.

Year 1 work:

Application/requirements thread. (Schmalz, Frank) Months 1-2: Work with DoD tactical systems experts to learn detailed requirements for in-the-field, low-power, mobile tactical embedded computing systems. Select appropriate application for implementation in adiabatic demonstration system.

Testing thread. (Frank, Ngo, Eisenstadt) Months 1-3: Order electronic and thermal testing & metrology equipment, validate it, design & build test setups. Apply test setups as needed by other threads.

Power supply thread. (Ngo, Frank, Fox, O) Months 1-6: Order electronic components, design & build adiabatic power supply, test & characterize stand-alone energy efficiency. Months 8-9: System integration of power supply with logic parts. Months 10-12: Document & deliver design.

Dummy chip thread. (Eisenstadt, Frank) Months 1-2: Obtain design tools. Design a very simple adiabatic chip (e.g. shift register) to validate the design & testing tools and the design process workflow. Months 3-5: MOSIS fabrication. Month 6: Testing.

Modeling thread. (Frank, Schmalz, etc.) Months 1-8: Refine present models of adiabatic power, performance, and cost-efficiency tradeoffs. Design and implement software analysis tools. Months 9-10: Further refinement. Months 11-12: Documentation & delivery

Conventional design thread. (Eisenstadt, Schmalz) Months 3-4: Design conventional chip for chosen tactical application, for comparison purposes. Months 5-7: Fabrication. Months 8-9: Testing & metrology.

Adiabatic design thread. (Eisenstadt, Frank, Schmalz) Months 3-4: Design adiabatic chip for chosen tactical application. Months 5-7: Fabrication. Months 8-9 testing & metrology. Months 10-12: Write up & deliver adiabatic design & detailed comparison of cost-efficiency of conventional & adiabatic designs for the chosen application.

MEMS thread. (Frank, Nishida) Months 1-3: Detailed research on performance characteristics of available MEMS switches, and analysis of potential cost-efficiency gains. Months 4-6: Investigate other advanced device technologies. Months 11-12: Documentation & delivery of results.

Year 2 option:

MEMS thread. (Frank, Nishida, Ngo) Months 1-2: If year 1 results are promising, design a fabricable MEMS-based power supply or other appropriate adiabatic systems component. Months 3-5: Have part fabricated (by commercial foundry or other research lab). Months 6-7: Testing of part. Months 8-9: System integration with improved adiabatic design, more testing. Months 10-12: Documentation & delivery of results.

Power supply thread. (Frank, Ngo) Months 1-6. Regardless of whether MEMS results from year 1 are promising, refine power supply design based on lessons learned from year 1. Test new design.

Adiabatic design thread. (Eisenstadt, Frank) Months 1-7: Refine adiabatic chip design based on lessons learned from year 1, fabricate, test,

System integration thread. (Eisenstadt, Frank, Ngo) Months 8-12: Create a comprehensive integrated system design encompassing both the logic part and the power supply, with real-world production in mind. Comprehensively test the integrated system using our demonstration parts. Document & deliver results.

Modeling thread. (Frank, Schmalz, etc.) Months 1-12: Refine models and software based on lessons learned from year 1 and ongoing work in year 2. Document & deliver improved software and models.

Year 3 option:

Modeling thread. (Frank, Schmalz, Ngo, Nishida, Fox, O) Create a detailed, comprehensive document surveying the potential cost-efficiency gains attainable with adiabatic technology, extrapolated into future technological environments where alternative low-power computing technologies might become available. Include impact of increasing leakage currents in scaled MOSFET technology. Include lifetime estimates for adiabatic technology advantages.

Application/requirements thread. (Schmalz, Frank) Months 1-2. Assuming year 1 & 2 results are successful, obtain detailed requirements for additional mobile tactical computing applications from DoD, and apply modeling software to determine for which additional applications adiabatic techniques can gain cost-efficiency.

Adiabatic design thread. (Eisenstadt, Frank) Months 3-12. Another round of adiabatic chip design, fabrication, & testing, for the new demonstration application. In parallel, further refinement of year 2 systems. Documentation & delivery of results.

Technology transfer thread. (Frank, Schmalz, Ngo, Eisenstadt) Throughout the year, work closely with DoD or industry contractors to fully integrate the demonstrated technologies into production lines for real tactical systems.

Summary of II E, III E: Comparison with other ongoing research.

The only major competing ongoing program in adiabatic circuits of which we are presently aware is the ACMOS group of Athas et al. at USC's Information Sciences Institute [9,10]. ISI's work is of high quality, and Frank's former group at MIT has worked with them on prior occasions. However, ISI's focus tends to be on the evolutionary, incremental application of adiabatic techniques within only selected portions of a processor - such as its buses or pad drivers only - which limits the maximum energy efficiency gains that can be attained, since the energy of the non-adiabatic portions of the processor comes to dominate. In contrast, the more thorough MIT/UF approach aims to progressively minimize all the different sources of energy dissipation, thereby offering better power/performance scaling, lower minimum energy, and with this proposed research program, better overall cost-effectiveness for energy-limited tactical applications.

Summary of II F: Organization chart.

Dr. Frank will coordinate and administer the whole project, and share responsibility for the primary deliverables with Drs. Eisenstadt, Ngo, and Schmalz. Drs. Fox, O, and Nishida will serve a somewhat smaller role, helping with modeling and advanced device research as needed..

Summary of III F: Proposers' Prior Accomplishments in Related Areas

Here is some relevant data for the primary team members:

Dr. Frank, our adiabatic circuits expert, recently (last year) completed his Ph.D. thesis work [1] on adiabatic circuits at MIT, in the research group that developed the first practical fully-adiabatic circuit style [5,6]. In his work, Frank discovered new results in scaling of reversible technology [2,4], designed the first fully-adiabatic universal processor [3], and helped design a reversible instruction set for a larger fully-reversible CPU []. Since his graduation from MIT, Frank has discovered a number of improvements to adiabatic circuit techniques, which will be published as they are implemented and tested during the course of the proposed project.

William R. Eisenstadt, our VLSI expert, received the B.S., M.S., and Ph.D. degrees in electrical engineering from Stanford University, Stanford, CA, in 1979, 1981, and 1986, respectively. In 1984, he joined the faculty of the University of Florida, Gainesville, FL, where he is now an Associate Professor. His research has been concerned with mixed-signal embedded IC testing and high-frequency characterization integrated circuit devices, packages, and interconnect. In addition, he is interested in large-signal microwave circuit and analog circuit design. He has over 20 years experience in VLSI design and architectures. Dr. Eisenstadt received the NSF Presidential Young Investigator Award in 1985.

Mark Schmalz, our tactical computing expert, has extensive experience in DoD-sponsored research programs and in mobile parallelized signal and image-processing systems. He has authored or co-authored over 95 research papers in open conference proceedings and journals.

Khai D. T. Ngo, our power systems expert, received a B.S. degree in Electrical and Electronics Engineering from California State Polytechnic University, Pomona in 1979, and an M.S. and Ph.D. degree in the same discipline from California Institute of Technology in 1980 and 1984, respectively. He was a Member of Technical Staff at General Electric Corporate Research and Development Center in Schenectady, New York from 1984 to 1988. He has been an Associate Professor in the Department of Electrical and Computer Engineering at the University of Florida since 1988. His current research interest includes the synthesis and control of power converters; power quality; low-power power electronics low-profile magnetics; power semiconductor devices and integrated circuits.

Summary of III G. Facilities.

The UF CISE department has an extensive network of Unix workstations suitable for programming or IC design. The ECE department has IC design software and lab space which can be used to design, build and test prototype systems. Actual silicon fabrication will be outsourced to MOSIS and other fab facilities as needed.

Summary of IV: Bibliography.

[1] Michael P. Frank, "Reversibility for Efficient Computing," Ph.D. Thesis, MIT, June 1999. A product of "Reversible Computing for Energy Efficient and Trustable Computation" (DARPA Scalable Computing Systems program contract #DABT63-95-C-0130). `http://www.ai.mit.edu/~mpf/rc/thesis/phdthesis.html`

[2] Michael P. Frank, Tom Knight, Norm Margolus, ‘‘Reversibility in optimal scalable computer architectures,’’ in Calude, Casti, Dineen, eds., *Unconventional Models of Computation* (proceedings of the First International Conference on Unconventional Models of Computation, Jan. 1998), pages 165-182, Springer, 1998. `http://www.ai.mit.edu/~mpf/rc/scaling_paper/scaling.html`.

[3] Michael P. Frank, Carlin Vieri, M. Josephine Ammer, Nicole Love, Norman H. Margolus, Thomas F. Knight, Jr., ‘‘A scalable reversible computer in silicon,’’ in *ibid*., pages 183-200. `http://www.ai.mit.edu/~mpf/rc/flattop/ft.html.`

[4] Michael P. Frank and Tom Knight, ‘‘Ultimate Theoretical Models of Nanocomputers,’’ *Nanotechnology* **9**(3):162-176, Sep. 1998. Also presented at the Fifth Foresight Conference on Molecular Nanotechnology, Palo Alto, CA, Nov. 1997. `http://www.ai.mit.edu/~mpf/Nano97/paper.html`.

[5] Saed G. Younis and Thomas F. Knight, Jr., "Asymptotically Zero Energy Split-Level Charge Recovery Logic," International Workshop on Low Power Design, 1994, pp. 177-182. `http://www.ai.mit.edu/people/tk/lowpower/low94.ps`

[6] Saed G. Younis, "Asymptotically Zero Energy Computing Using Split-Level Charge Recovery Logic," Ph.D. Thesis, MIT, 1994.

[7] Carlin J. Vieri, “Reversible Computer Engineering and Architecture,” Ph.D. thesis, MIT, 1999.

[8] Paul M. Solomon and David J. Frank (IBM), "Power Measurements of Adiabatic Circuits by Thermoelectric Technique", Symposium on Low Power Electronics, pp. 18-19, 1995.

[9] N. Tzartzanis, W. Athas, Clock-Powered CMOS: A Hybrid Adiabatic Logic Style for Power-Efficient Computing, 20th Anniversary Conference on Advanced Research in VLSI, IEEE Computer Society Press, Mar. 1999, pp. 137-151.

[10] W.C. Athas, L."J." Svensson, J.G. Koller, N. Tzartzanis, E. Chou, Low-Power Digital Systems Based on Adiabatic-Switching Principles, in the IEEE Transactions on VLSI Systems, pp 398-407, Dec. 1994. Also see http://www.isi.edu/acmos/acmosPapers.html

One-page summary of Volume II: Cost Proposal

The following are rough estimates, for proposal abstract purposes. The figures in the final proposal may vary from this somewhat but will not exceed $500K/year. Figures are rounded to the nearest $1K.

Cost Category	Year 1	Year 2 (opt)	Year 3 (opt)	Totals
Faculty salary & benefits:	$125K	$123K	$121K	$ 370K
Student salaries & tuition:	$ 91K	$ 95K	$ 98K	$ 285K
Equipment:	$ 70K	$ 50K	$ 50K	$ 170K
Travel (domestic):	$ 14K	$ 14K	$ 14K	$ 42K
Chip fabrication:	$ 40K	$ 40K	$ 40K	$ 120K
Computer maintenance:	$ 8K	$ 8K	$ 8K	$ 24K
TOTAL DIRECT COSTS:	**$349K**	**$331K**	**$332K**	**$1,012K**
Indirect costs (44% of direct except equipment + tuition):	$116K	$116K	$116K	$ 348K
TOTAL COST:	**$466K**	**$447K**	**$448K**	**$1,360K**

Salary notes: Drs. Frank and Schmalz are at 25% full-time equivalent, Dr. Eisenstadt at 30%, Dr. Ngo initially at 25% but decreasing by 5%/year, Dr. Fox at 5%, and Dr. O at 10% for 9 months/yr. Dr. Nishida will consult informally at no cost. Students are 3 graduate students at 50%, 1 at 33%, and 2 at 25%.

Equipment notes: Year 1 includes calorimetry equipment and a new high-precision oscilloscope for sensitive energy dissipation measurements. Years 2 and 3 include anticipated costs for MEMS components. All years include a lump sum of $35K for incremental purchase of miscellaneous electronic test equipment, electronic components, tools, and computer equipment as needs arise.

Travel notes: Estimated $1,000 for air travel, hotel, and other fees for each of 2 domestic trips per faculty member per year, for purposes of attending conferences and/or PI meetings