Design for MOSIS Educational Program (Research)

Project Title:

A fully-adiabatic logic test chip based on the 4-phase 2LAL (2-Level Adiabatic Logic) family, with integrated MEMS postprocessing for high-quality energy recovery

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Project Description

We propose to design and fabricate a fully adiabatic CMOS logic test chip, for purposes of demonstrating operation at ultra-low (on the order of 10's of picowatts per gate) power levels, while maintaining better performance (and even cost-performance) than conventional fully-irreversible static CMOS operating at the same power level would be able to achieve (even with voltage scaling) in the same process. This chip will be the first demonstration die to utilize the 2LAL logic family, a novel fully-adiabatic logic family invented at UF. The 2LAL family is distinguished from prior adiabatic logic families in that it fully maintains truly-adiabatic operation throughout its cycle. For example, it completely avoids the dissipative "squelch" events which occur whenever transistors are switched off while they are still carrying current, an event that occurs frequently in many of the supposedly-adiabatic logic families in the low-power design literature (which are thus not actually fully adiabatic). At the same time, 2LAL requires only a small number of externally-supplied driving signals, has minimal gate delay and cycle time for a given adiabatic transition time, and is also reasonably hardware efficient, requiring only roughly 4× as many transistors per gate as regular static CMOS.

A 2LAL chip would be particularly well suited to be driven by a resonant trapezoidal waveform generator with a 25% rise time, such as the one that we are concurrently designing in the context of the AdiaMEMS project at UF, which is supported by a small grant from SRC and a MEMS process donation from Robert Bosch corp. The combined chipset (Bosch MEMS chip plus MOSIS TSMC CMOS) would allow students to empirically verify low total system power dissipation for the combined (CMOS logic + MEMS power supply) chipset, which has not previously been done. Most previous demonstrations of low-power adiabatic logic have discounted the energy dissipated in the power supply, which is generally a significant part of the total system power dissipation.

In this project we plan to integrate the MEMS power supply together with CMOS adiabatic logic on the same die using special MEMS post-processing steps developed by our group.

System Design and Simulations

We have already designed and simulated simple 2LAL logic circuits in Cadence, using UF's TEC lab installation of the process model libraries for the TSMC 0.18µm process. Proper functionality and low power dissipation of the circuits has been validated in simulations using standard device models using Cadence and a custom simulator in MATLAB.

At present, we have designed a suite of basic logic gates and adder cells, and are currently in the process of building up our design libraries to include higher-level elements such as shift registers, wide adders and multipliers, register files, sequential pipelines, and systolic arrays of arithmetic units. Some set of these higher-level elements (to be determined) will be included on our proposed test chip.

We have also implemented deep-submicron MOSFET models in MATLAB using the standard set of equations taken from the documentation of BSIM3 (MOSIS level 49),

BSIM4, and the Cadence Spectre models, and plugged in the level 49 model parameters for sample TSMC18 process runs that were supplied on the MOSIS website.

These MATLAB models are needed as components of a higher-level system-design optimization code we are building, which will choose operating voltage, body bias, and operating frequency appropriately so as to maximize the system-level figures of merit (such as cost-performance at ultra-low-power levels) which we are interested in. The optimization is non-trivial because of the interactions between the threshold voltage, subthreshold leakage current, and on-current. Traditional software for performing these optimizations cannot be used, since the tradeoffs are different for adiabatic logic. In fully-adiabatic logic, the switching power dissipation is so low that leakage becomes the dominant mechanism of power dissipation at much higher operating frequencies than if traditional switching were used. Therefore, an accurate model of subthreshold conduction is critical for accurately estimating the total power dissipation of our circuits, even at reasonably high frequencies.

Whether or not the latest processes available through MOSIS would support a high enough on/off current ratio in order to support our ultra-low-power application scenario was initially a matter of some concern. Fortunately, our MATLAB model (which has been roughly validated against Cadence for other processes) indicates that even in TSMC 0.18 operating at a logic swing voltage V_{dd} of only 1V (for low power), an on/off ratio on the order of 10^{10} is still supported. Based on this, our proposed adiabatic chip ought to be able to achieve a theoretical boost in power-performance (compared with conventional logic with the same process and V_{dd}) on the order of roughly the square root of this number, or 10^5, before leakage becomes a limiting concern.

(When running at the optimal frequency, $\sim 10^5$ times lower than the peak I/Q frequency of the device, the adiabatic switching energy losses per cycle will be $\sim 10^5$ times lower than the peak value, while leakage energy losses per cycle will be $\sim 10^5$ times higher than the normal value, and so the two numbers will "meet in the middle" of the 10^{10} range, and thus will be roughly comparable.)

Even when compared against more traditional low-power techniques such as optimized voltage scaling in the sub-threshold regime, detailed simulations reveal that roughly a 50× boost in power-performance is still achievable by the adiabatic approach compared with voltage-scaled CMOS.

Based on these modeling results, it was deemed feasible to pursue the fabrication of an ultra-low-power 2LAL test chip in the TSMC 0.18 micron process, which is the focus of the present proposal.

The TEC lab at UF is already using the TSMC 0.18 micron libraries for other projects, and the TEC lab owners have provided us access to their facilities for our project.

Fabrication Process

The TSMC 0.18 micron process was selected since it is the smallest well-characterized process presently available through MOSIS, and it apparently still provides the sufficiently high on/off ratios that we require. We only need the CLO18 version of the process, since we are not planning to do mixed-signal design on-chip initially. (Our circuits are fully digital.)

Since in our project we are attempting to minimize power, we will be operating in a regime where subthreshold power is significant, and so we may also want to adjust threshold voltages as needed in order to optimally trade off subthreshold power against on-current. If the process does not offer selectable-V_t devices (e.g. through variation of dopant concentrations), then we may instead attempt to adjust the device thresholds on the lab bench by varying the N-well and P-well body bias (thus invoking the body effect), while of course still staying within the limits required for correct device functionality.

We are planning to post-etch MEMS structures onto a reserved area of our die using a process for this that has been developed at UF and that has already been used extensively on other projects.

Pads

We may wish to include some custom output pads that use adiabatic switching (rather the usual static-CMOS buffering) to drive the output pins, so that a significant output signal may be generated without compromising ultra-low-power operation. (The other, non-adiabatic output pads will need an option to disable them when measuring low power.)

Packaging Requirements

Similarly, we would like to minimize the parasitic characteristics (particularly capacitance) of the I/O bonding wires, package-internal wiring, and the package pins. In fact, it might be a good idea if a few of the dies were provided unpackaged, so that we could characterize the small signals produced by individual MEMS resonators in the absence of packaging-related parasitics.

Estimated Project Size

The estimated die size for this project is 2.6 mm × 2.6 mm (7 mm^2).
(The discount price for this size die in TSMC CL018 as of 03/24/04: $22,400.)

Test and Characterization Plans

There will be several phases of testing: (1) pure functionality test, (2) power dissipation test under ideal external drive signals, (3) post-MEMS-etch logic regression test, (4) MEMS resonator testing, and (5) system power dissipation test when coupled with MEMS resonator.

(1) Pure functionality test. On the lab bench, the 2LAL chip will be driven using 4 simple square-wave (50% duty cycle) clock inputs provided by an external signal generator, with separate body bias inputs set to the ordinary 0V (N-well) and V_{dd} (P-well) levels initially. A logic analyzer will be used to provide input data sequences. Signals from critical test points within the circuit will be routed to regular (nonadiabatic) output pads which will be switched on so that we can observe the output signals on a scope. Correct functionality will be characterized, as well as gate delays for the original gates. A wide range of V_{dd} levels (but none

much above 1.8V, to avoid shorting out the gate electrodes) and operating frequencies will be tried, so as to characterize the maximum operating frequency supported at each voltage level. In additional, alternate body-bias levels will be tried, in order to verify the variability permitted while maintaining correct function. Results will be compared against predictions from our MATLAB device model and Cadence simulations, to validate these modeling/simulation tools.

(2) Ideal-source power dissipation test. In this test, the square-wave clock will be replaced with an ideal trapezoidal clock (50% duty cycle, 25% rise time), and chip power dissipation will be measured as a function of frequency, and compared with predictions. (We plan to measure the power dissipation using a sensitive thermoelectric calorimeter, which we will build and validate prior to this test.) A variety of settings for V_{dd} and body bias will also be tried and results compared to simulations.

(3) MEMS post-etch regression testing. After MEMS structures are etched onto the die by our post-processing steps, tests (1) and (2) will be repeated to ensure that logic functionality remains undisturbed.

(4) MEMS resonator testing. We will drive the post-etched resonators using small sinusoidal AC input signals provided by a signal general, with output signals routed to linear op-amp driven output pins. We will validate the output waveform's shape, resonance frequency, and the quality factor of the resonator. This data will be collected at a small range of frequencies accessed via electrostatic tuning of the resonant frequency..

(5) System power dissipation test. In this test, configuration input signals will be set to couple the adiabatic logic to the MEMS resonators, and turn off non-adiabatic output pads. The chip will be placed within the calorimetry setup. A small ideal sinusoidal signal from a waveform generator (outside the calorimeter) will pump the MEMS resonator at its resonant frequency. Total system power dissipation will be measured within the narrow range of frequencies accessible via electrostatic tuning of the resonant frequency of the MEMS part. Also, as a cross-check, the RMS power contained in the AC signal driving the system will be measured using standard inductive probes, and should be at a comparable level to the calorimetry-derived power.