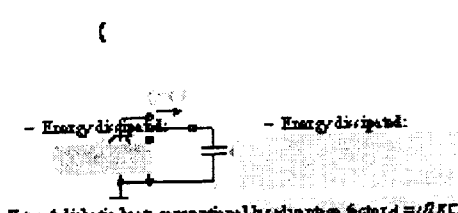


### Conventional vs. Adiabatic Charging

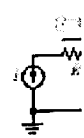
For charging a capacitive load  $C$  through a voltage source  $V$

- Conventional charging:
  - Constant voltage source
- Ideal adiabatic charging:
  - Constant current source



### Adiabatic Switching with MOSFETs

- Use a voltage ramp to approximate a current source.
- Switch under condition that MOSFET gate voltage  $V_g > V + V_T$  during ramp.
- Can discharge the load later using a similar ramp.



$t > RC \Rightarrow$  [shaded box]

$t < RC \Rightarrow$  [shaded box]

Exact formula:  
 given a peak fraction  $\alpha = E_{RC}$

FIGURE 1

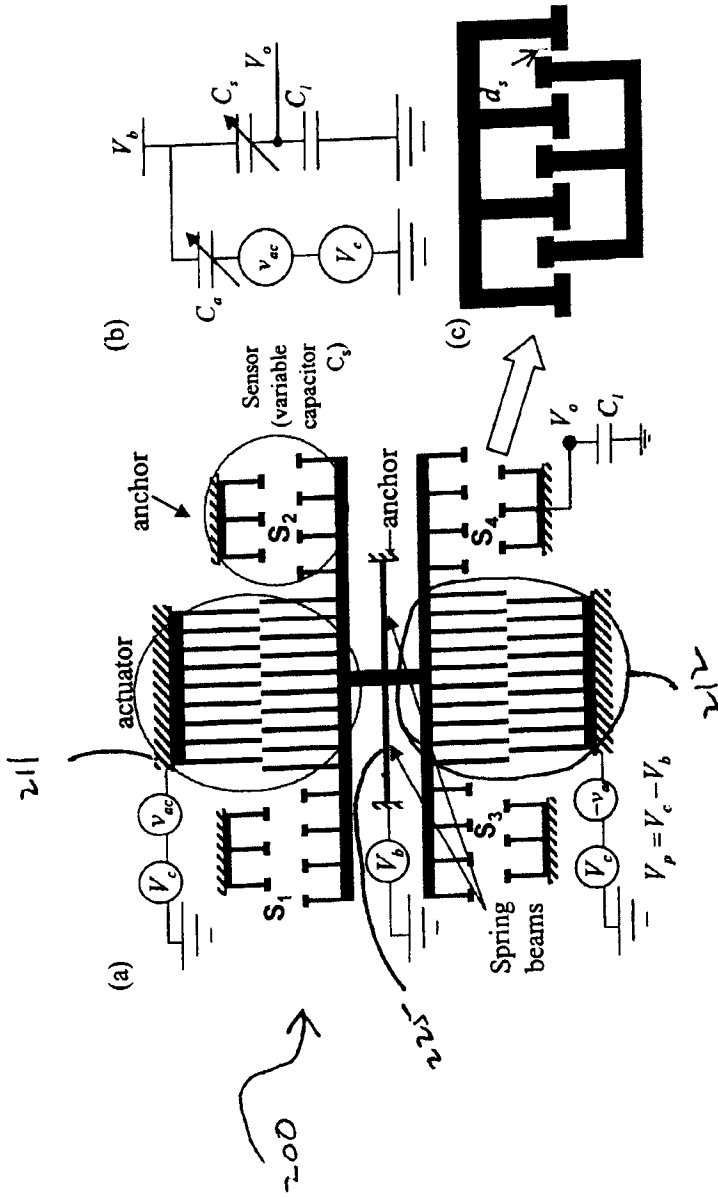
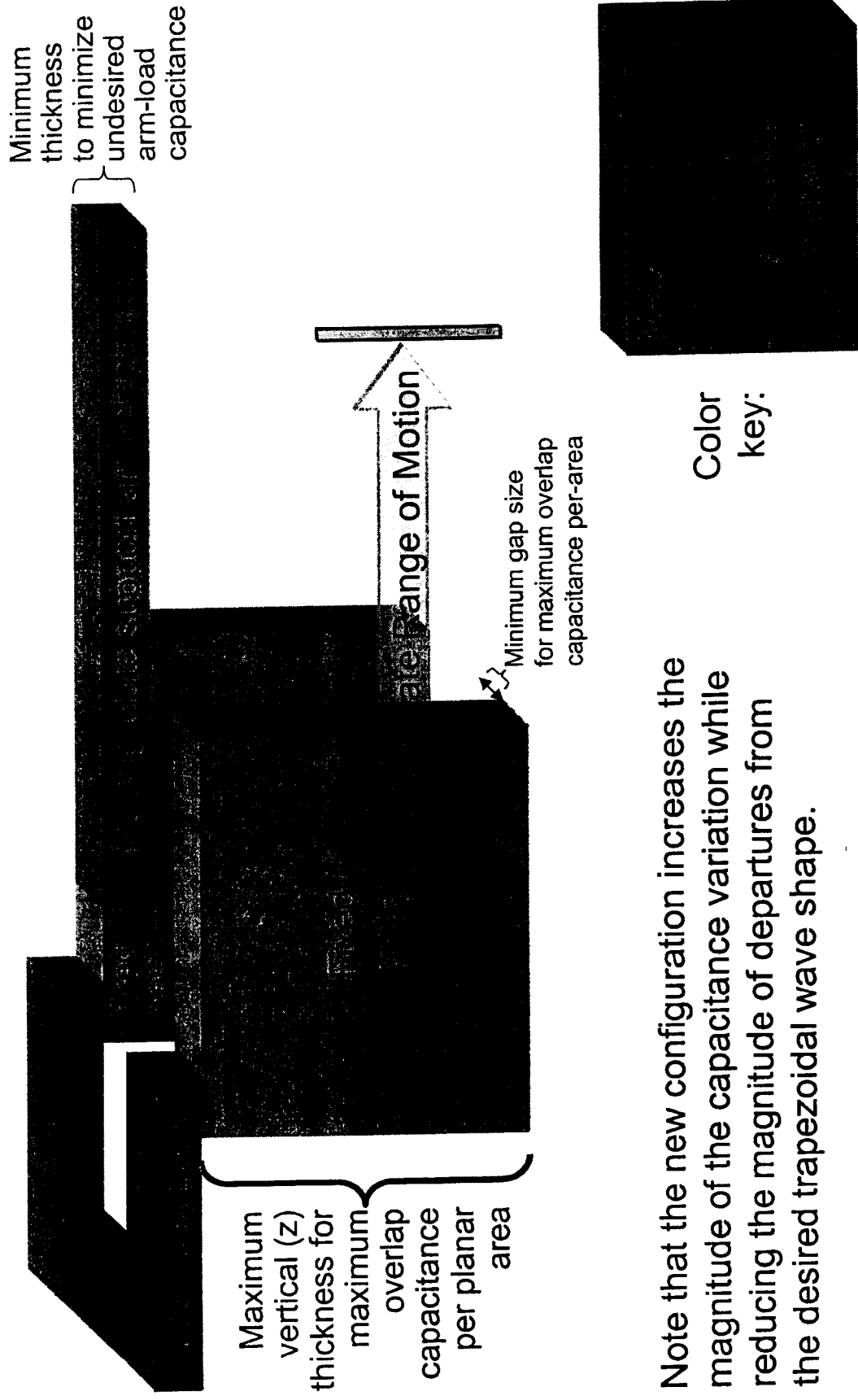


FIGURE 2

# New Comb Finger Shape I

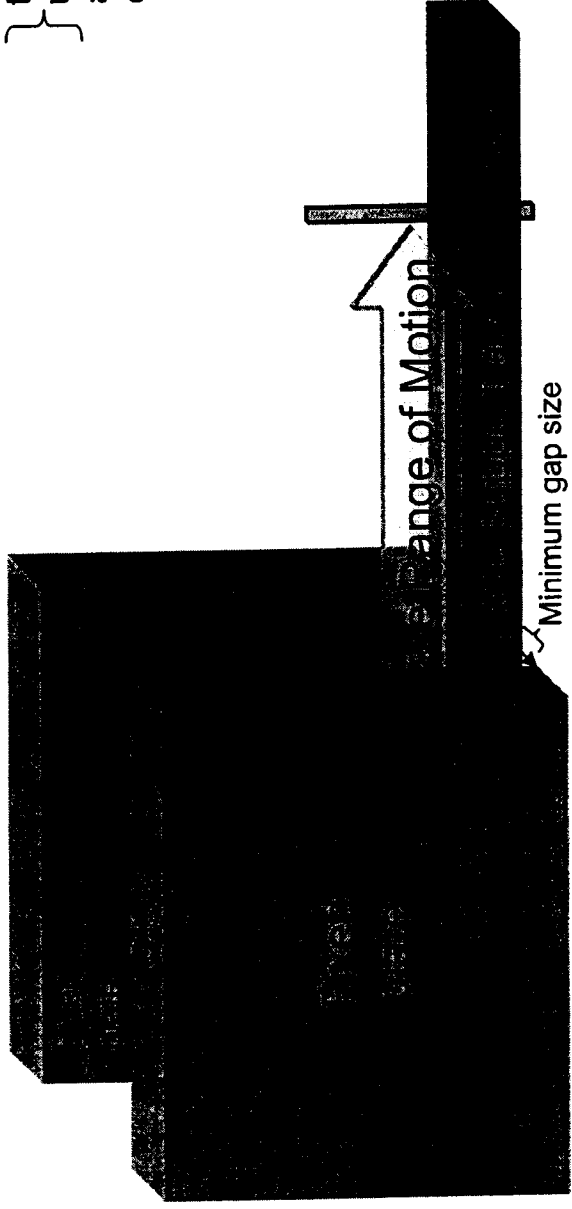


Note that the new configuration increases the magnitude of the capacitance variation while reducing the magnitude of departures from the desired trapezoidal wave shape.

FIGURE 3A

# New Comb Finger Shape II

Minimum thickness to minimize undesired arm-load capacitance



Maximum vertical (z) thickness for maximum overlap capacitance per planar area

Range of Motion

Minimum gap size for maximum overlap capacitance per-area

Note that the new configuration increases the magnitude of the capacitance variation while reducing the magnitude of departures from the desired trapezoidal wave shape. In addition, the structures are made of silicon

Color key:

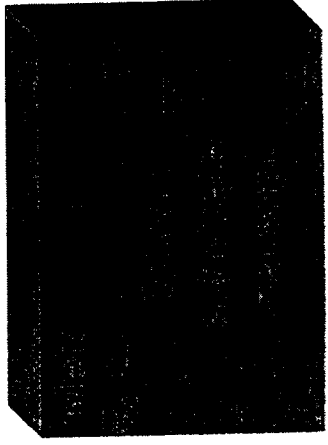
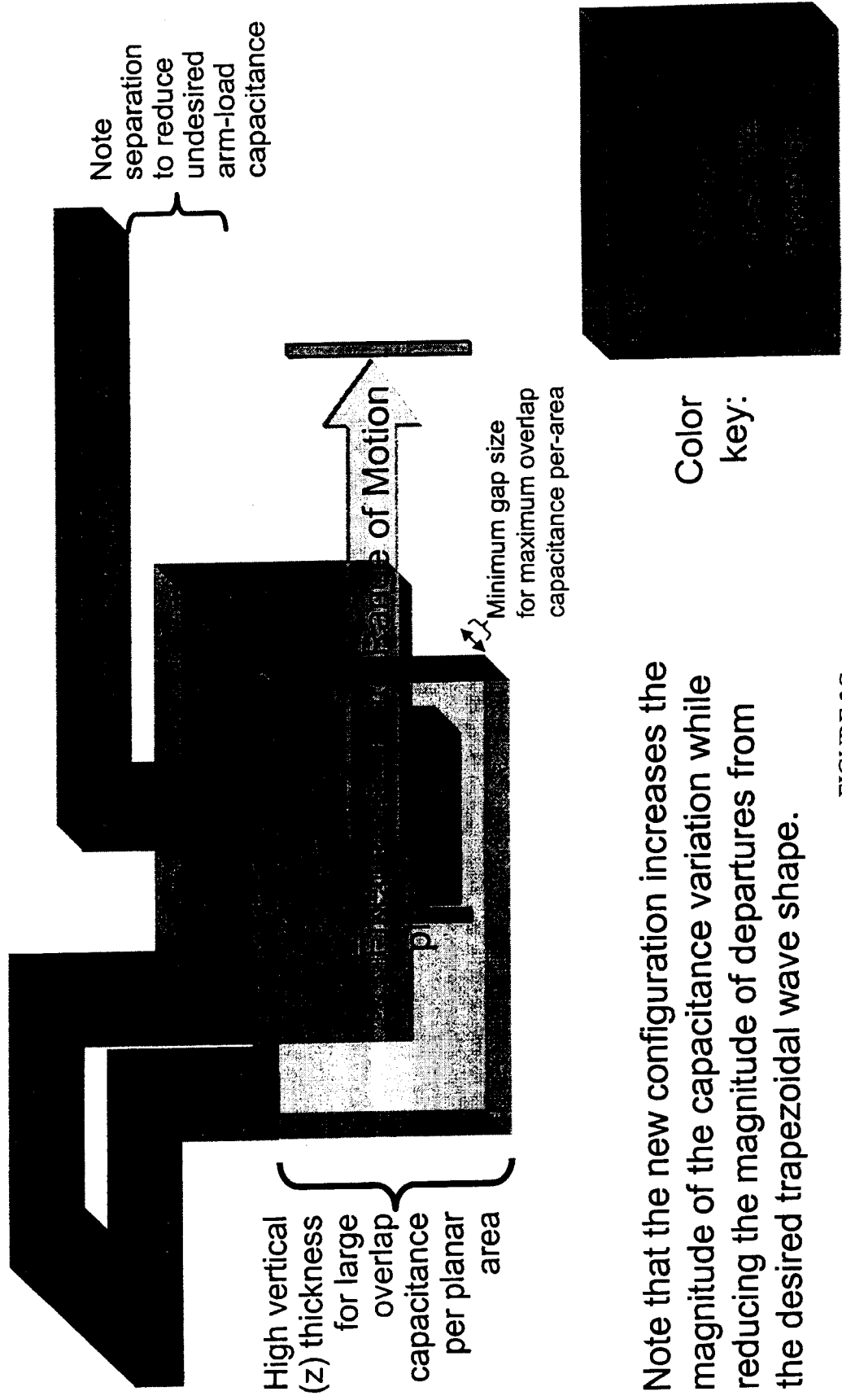


FIGURE 3B

# New Comb Finger Shape III

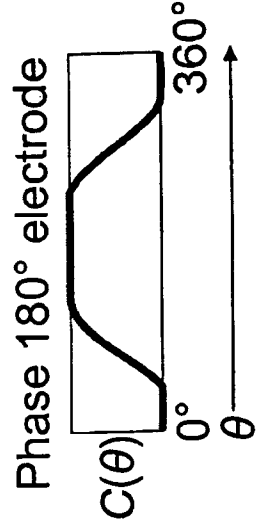
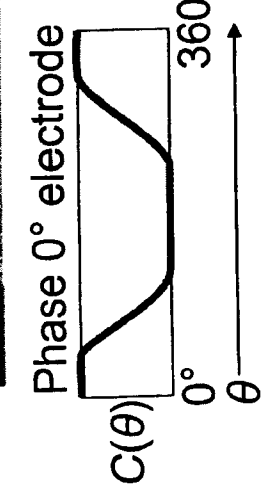
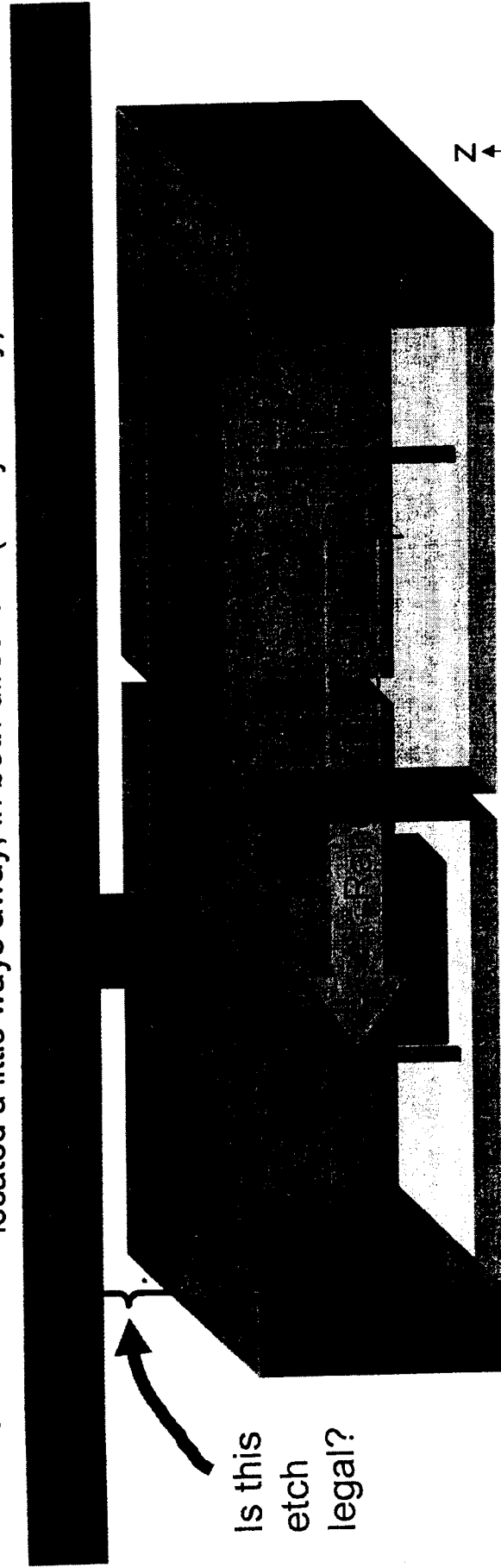



Note that the new configuration increases the magnitude of the capacitance variation while reducing the magnitude of departures from the desired trapezoidal wave shape.

FIGURE 3C

# New Comb Finger Shape IV


 Arm anchored to nodal points of fixed-fixed beam flexures, located a little ways away, in both directions (for symmetry)
 




 Repeat interdigitated structure arbitrarily many times along y axis, all anchored to the same flexure

Or, if we can do the structure on the previous slide, then why not this one too? Or, will there be a problem etching the intervening silicon out from in between the metal/oxide layers and the bulk substrate?

FIGURE 3D

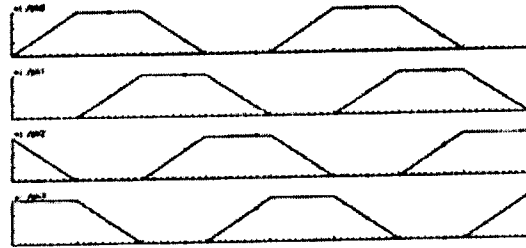


FIGURE 4

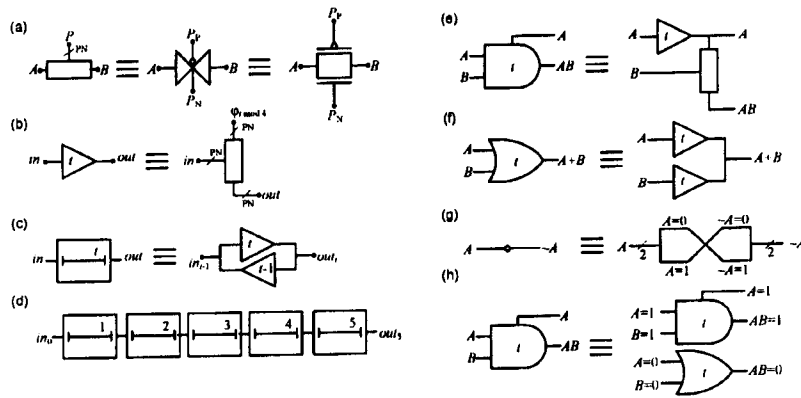


FIGURE 5

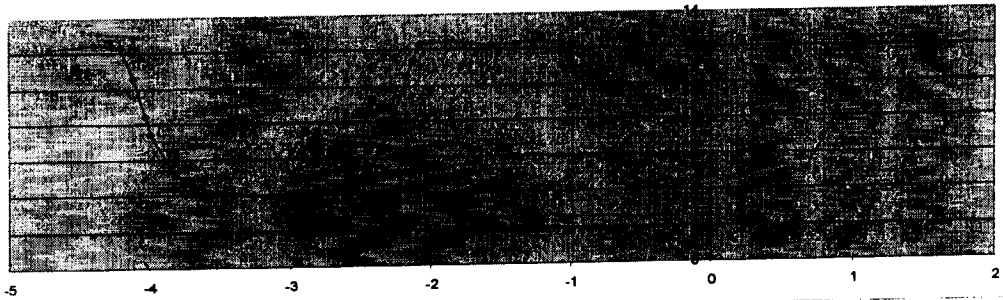


FIGURE 6



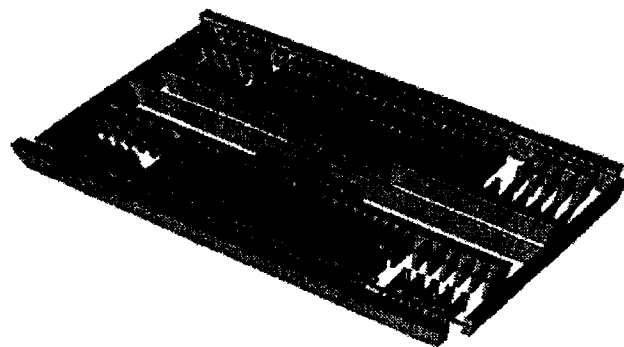


FIGURE 7

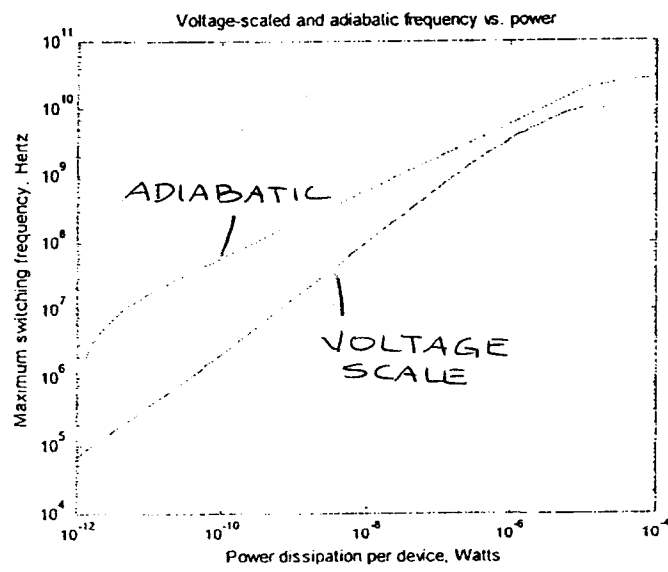


FIGURE 8