HIGH-*Q* MEMS RESONATORS AND ADIABATIC LOGIC CIRCUITS USING THE SAME

CROSS-REFERENCE TO RELATED APPLICATIONS

[0001]   Not applicable.

STATEMENT REGARDING FEDERALLY SPONSORED

RESEARCH OR DEVELOPMENT

[0002]   Not applicable.

FIELD OF THE INVENTION

[0003]   This invention relates to MEMS waveform generators which utilize displacement controlled varactors and circuits which are driven by AC signals provided by such generators, including adiabatic logic circuits.

BACKGROUND OF THE INVENTION

[0004]   The power-performance efficiency of traditional non-adiabatic circuits is reaching its limits. Supply voltages are generally already about as low as they can get being on the order of 1V. Voltages far lower than this lead to poor transistor on/off ratios at room temperature, and significant problems with subthreshold conduction and the resulting leakage power dissipation. Even if subthreshhold conduction and resulting leakage could be substantially avoided, such as by operating at a deeply sub-ambient temperature, still the fundamental thermodynamic limit of $kT\ln(2) \approx 18$ meV for the energy dissipation of an irreversible digital operation (bit erasure)

given a room-temperature external environment is only about 30 years away, if present trends continue. This thermodynamic limit is not possible to avoid except through the use of reversible "adiabatic" computing. Thus, over time, it is expected that a fully-adiabatic and logically-reversible design style may gradually become the norm for the majority of high-performance and power-limited computing applications.

[0005]   The field of adiabatic circuits comprises low-power digital design techniques that are based on carrying out most charge transfers across transistors in a gradual and controlled or quasistatic fashion, such that the electron "gas" in the circuit always remains close to a local equilibrium state. Such operation minimizes entropy generation and thus the energy dissipation of the overall circuit. Carrying out charge movement adiabatically requires that logic gates be driven by power supply signals that are AC rather than DC, and that have a quasi-trapezoidal (flat wave peaks and troughs, and gradual transitions) waveform shape rather than square wave (with steep transitions) or sinusoidal (curved peaks and troughs). Such trapezoidal wave shapes are required in order to ensure that universal digital logic can be carried out while still obeying the following constraints which are recognized as requirements for quasistatic operation:

     i.   never pass current through a diode (or diode-based transistor, such as a bipolar transistor); such as use FETs only,

     ii.   never turn on a FET transistor if there is a voltage across it ($V_{DS} \neq 0$), and

     iii. never turn *off* a FET transistor if there is a current through it ($I_{DS} \neq 0$).

The importance of adiabatics can be appreciated by first considering the task of changing the logic value that is stored on a circuit node of capacitance C, in ordinary voltage-coded logic, by transitioning the node through a voltage swing of $V = |\Delta V| = V_{dd}$. If the node is transitioned by connecting it to a constant-voltage power supply at the desired level, this leads to an

unavoidable energy dissipation of $E_{diss} = \frac{1}{2}CV^2$. In contrast, if instead the node is connected to a power supply which is initially at the same voltage level, but which subsequently ramps to the new level linearly over a time interval t as shown in FIG. 1, the energy dissipation is given by:

$$E_{diss} = s(1 + s(e^{-1/s} - 1)) \cdot CV^2 \quad (1)$$

where $s = RC/t$ is the speed fraction, the speed of the ramping event compared with the RC time constant of the circuit; R is the effective resistance along the charging path. When $t >> RC$, Equation (1) approaches $E_{diss} \approx CV^2 s$, in other words, the energy savings factor approaches $t/2s = t/2RC$ compared with traditional switching. Thus, the energy dissipation can be reduced by an arbitrarily large factor as the charging time is increased.

[0006]   At first it may seem that increasing the time for a logic transition is impractical, since what is desired is generally high performance (or as high as possible) at low power, not just low power. But in many situations it is the power dissipation, and not the RC time constant of the devices, which limits the maximum practically obtainable switching frequency. For example, for traditional switching events occurring, once per cycle at frequency f, the average power dissipation is given by $P_{trad} = \frac{1}{2}CV^2 f$. Now consider performing those very same switching events adiabatically over a ramp time that is $\frac{1}{4}$ of a full clock cycle, that is $t = 1/4f$. Since the adiabatic energy dissipation of each switching event is $E_{diss} = CV^2 s = CV^2 RC/t = 4CV^2 RCf$, at one such transition per cycle, the average power is $P_{adia} = E_{diss}f = 4CV^2 RCf^2$, lower than the conventional design by a factor of $1/8RCf$.

[0007]   Suppose now that the application requirements impose constraints to switch individual gates at an average power level of only $P_{trad} = P_{adia} = P$. The maximum frequencies f_{trad} and f_{adia} at which this low of a switching power could be achieved is now compared in

adiabatic versus traditional solutions. Since $P = \frac{1}{2}CV^2 f_{\text{trad}}$, $f_{\text{trad}} = 2P/CV^2$, while since $P = 4CV^2 RC f_{\text{adia}}^2$, solving for f_{adia} gives:

$$f_{adia} = \sqrt{\frac{P}{4CV^2 RC}} = \frac{1}{2CV}\sqrt{\frac{P}{R}} \, . \, (2)$$

So the speedup factor $F_{\text{su}} = f_{\text{adia}}/f_{\text{trad}}$ that can be gained through adiabatic switching is given by:

$$F_{su} = \frac{f_{adia}}{f_{trad}} = \frac{(1/2CV)\sqrt{P/R}}{2P/CV^2} = \frac{V}{4\sqrt{PR}} \, . \qquad (3)$$

[0008]   Thus, given the voltage swing V and charging-path resistance R, the adiabatic speedup increases (by a square-root factor) as the allowed power level P becomes smaller. Since the effective resistance R can be approximated as $R \approx V/I$, where I is the current along the charging path when the total voltage drop along it is V, the speedup factor shown in Equation (3) can be simplified further, to the form $F_{su} = \frac{1}{4}\sqrt{IV/P} = \frac{1}{4}\sqrt{P_{full}/P}$, where $P_{\text{full}} = IV$ is the "full throttle" power dissipation along the charging path when the voltage drop along it is the full logic swing, and P is (still) defined as the maximum power dissipation that can be tolerated given the application constraints.

[0009]   So, for example, suppose a conventional design that, when operated at the top theoretical speed determined by its electrical characteristics (ignoring power), would dissipate 1,600 times as much power as is actually allowable in some applications. Then in principle, an adiabatic version of that circuit could run $\frac{1}{4}\sqrt{1,600} = 10$ times faster than the conventional one under that power constraint. The long-term value of the adiabatic approach is that, as devices start running up against energy-dissipation limits while they continue to get cheaper, the needed

power reduction factors P_{full}/P will get larger, and so the potential speed advantage of adiabatics will increase.

[00010] The above description did not account for other sources of power dissipation, such as current leakage across nominally turned-off devices. Also, it was assumed that the circuit complexity was unchanged by the transition to adiabatic switching.

[00011] In a more complete analysis which takes these factors into account, P_{lk} represents the average leakage power dissipation per logic node, and O_{adia} represents the hardware overhead (blowup) factor of the adiabatic design. Then, the speedup factor is instead given by

$$F_{su} = \frac{\sqrt{P_{full}\left(\frac{P}{O_{adia}} - P_{lk}\right)}}{4(P - P_{lk})} \qquad (4)$$

which is maximized at the power level $P = P_{lk}(2O_{adia} - 1)$, in which case the speedup is

$$F_{su} = \frac{1}{4}\sqrt{\frac{P_{full}/P_{lk}}{O_{adia}(O_{adia}-1)}} \approx \frac{1}{4} \cdot \frac{\sqrt{R_{on/off}}}{O_{adia}} \qquad (5)$$

where $R_{on/off} = P_{full} / P_{lk} = I_{on}/I_{off}$ is the on-off current ratio of the device technology, and where we have noted that $O_{adia}(O_{adia}-1) \approx O_{adia}^2$ when $O_{adia} \gg 1$ (as it usually is).

[00012] The on-off ratio itself varies with the device technology, but it can be as high as $R_{on/off} = e^{V/\varphi_T}$, where $\varphi_T = kT/q$ is the thermal voltage (~26 mV at room temperature), for the case of surround-gate devices operated in the subthreshhold regime. This yields adiabatic speedups as high as $F_{su} \approx e^{V/\varphi_T}/4O_{adia}$; this is >1 as long as $V > 2\varphi_T \ln(4O_{adia})$. In fact, that these potentially large speedups can justify staying at operating voltages that are high enough to keep $R_{on/off}$ large. Note that this only requires small (logarithmic) increases in device voltages; the energy hit from the slightly higher voltage can be easily outweighed by the advantages of adiabatic switching. It can be concluded that moving to ever-tinier devices (which require ever-lower voltages) is not,

in the end, always beneficial for maximizing power-performance, or even overall system cost-efficiency.

[00013]   As demonstrated above, given a fixed constraint on operating power, adiabatics can offer a performance advantage compared with traditional circuits. A cost-performance advantage can also be provided. The raw hardware cost of an adiabatic solution is increased by a factor of O_{adia} as well as by additional factors discuss below. As long as $V > 4\varphi_T \ln(4O_{\text{adia}})$ it can be shown that there is still a cost-performance advantage from adiabatics. The small increase in device size (and cost) necessitated by the slightly (logarithmically) higher voltage level is overwhelmed by the (exponentially larger) performance gain from energy-efficient adiabatic operation.

[00014]   A final issue excluded from the previous discussion is that for some applications the adiabatic overhead factor O_{adia} may actually need to increase as the power requirements become ever more stringent. The constraint of logical reversibility generally causes the space and time requirements of known algorithms to increase, as the fraction of computational operations that are performed irreversibly is decreased. However, an even more detailed analysis that accounts for this effect reveals that, even when accounting for the increasing overheads, the power-performance and cost-performance of adiabatic logic still beats conventional approaches over time, as the device manufacturing process becomes more cost-efficient and energy increasingly dominates the total cost.

[00015]   Power supply considerations for adiabatic operation are now examined. An adiabatic transition transfers an amount of static electrical energy given by $E_{\text{trans}} = \frac{1}{2}CV^2$ onto or off of a capacitor, while dissipating only $E_{\text{diss}} = CV^2 s$ of this energy to heat, where $s = RC/t$ is the relative switching speed. Therefore the Q factor of this process is $Q_{\text{adia}} = E_{\text{trans}}/E_{\text{diss}} = 1/2s$. The energy

transferred comes from (or goes to) some external energy-recovery element, which also has a Q factor Q_{ext}. Since the total dissipation $E_{dtot} = E_{trans}(1/Q_{adia} + 1/Q_{ext})$ the overall Q factor is $Q = (Q_{adia}^{-1} + Q_{ext}^{-1})^{-1}$, that is, it is limited to at most the Q_{ext} of the external element. Therefore, achieving all the above predictions requires an external resonant element with a sufficiently high Q factor.

[00016] The energy savings provided by adiabatic circuits is limited by the energy efficiency of the external element that generates the trapezoidal waveform. Ideally this generator element should be a resonator (energy-recovering oscillator) with a high Q factor. Generating an accurate quasi-trapezoidal signal with a conventional electronic resonator, such as using an LC-filter ladder circuit, is difficult, as very flat-topped signals (with low ringing amplitudes) require a substantial number of different Fourier components (modes) whose resonant frequencies and amplitudes must be precisely tuned. Moreover, if the required inductors and capacitors for the LC oscillator are fabricated on-chip, rather than being discrete components, they generally suffer from a low Q factor (typically only in the tens) due to the low inductance values and high parasitic substrate coupling of the low-coil-count integrated spiral or helical inductors that can be fabricated on-chip using currently available fabrication processes.

BRIEF DESCRIPTION OF THE DRAWINGS

[00017]   A fuller understanding of the present invention and the features and benefits thereof

will be accomplished upon review of the following detailed description together with the

accompanying drawings, in which:

[00018]   Figure 1 shows the energy dissipation of conventional versus adiabatic logic

transitions.

[00019]   Figure 2(a) –(c) shows a top view an exemplary MEMS resonator layout according to

an embodiment of the invention when the movable resonator beam is in its rest position, an

equivalent resonator circuit, and the position of the a sensor the resonator when the resonator

beam is at its maximum amplitude position, respectively.

[00020]   Figures 3(a)-3(e) show exemplary alternate comb finger shapes, according

embodiments of the invention.

[00021]   Figure 4 shows clock/power supply rails for an adiabatic logic family referred to as

2LAL. The rails consist simply of 4 trapezoidal voltage waveforms φ_0-φ_3, each with 50% duty

cycle and 25% transition time, at relative phases of 0°, 90°, 180° and 270°.

[00022]   Figure 5(a)-(h) show basic 2LAL notation and gates. Figure 5(a) shows a parallel

nFET/pFET pair whose control signal P is implicitly always a dual-rail pair of active-high (N)

and active-low (P) logic signals. Figure 5 (b) shows a 4-transistor 2LAL buffer for dual-rail

pulsed signals consists of two parallel transmission gates controlled by the input, passing a

power-clock signal $\varphi_{t\,mod\,4}$ and (implicitly in this drawing) its complementary, 180°-out-of-phase

signal $\varphi_{t+2\,mod\,4}$. Figure 5 (c) shows an 8-transistor adiabatic delay element that adiabatically

moves an input pulse @*t*-1 to an output pulse @*t*. Figure 5(d) shows delay elements with subsequent tick numbers can be chained together forming a shift register for input pulses. Figure 5(e) shows an AND gate for pulses (8 transistors) that consists of two transmission gates in series. Its internal node must be explicitly recognized as an extra output to maintain reversibility. Figure 5(f) shows an 8-transistor OR gate for pulses that consists of simultaneous transmission gates in parallel. Figure 5(g) shows a zero-delay, zero-transistor, non-amplifying NOT bubble implemented using quad-rail signaling; logic signal *A* is implemented as a pair of pulse signals, named *A*=0 and *A*=1. Figure 5(h) illustrates that when fed a quad-rail input signal an AND gate icon denotes a 16-transistor parallel pair of an AND and an OR (the latter to compute the *AB*=0 pulse).

[00023]   Figure 6 shows is a simulated output waveform from a MEMS resonator according to the invention. A refinement of the comb finger shape, together with additional compensating structures, is expected to further improve the wave shape to bring it even closer to an ideal trapezoidal waveform.

[00024]   Figure 7 is a 3D model of a complete resonator design presently being fabricated in a post-CMOS MEMS process starting with a Taiwan Semiconductor Manufacturing Company (TSMC) 35 micron die.

[00025]   Figure 8 shows simulation results based on an optimization analysis using a standard device model for confirming the performance advantage in terms of the maximum frequency vs. power dissipation provided by adiabatic circuits using resonators according to the invention, as compared to a conventional voltage scaled circuit.

DETAILED DESCRIPTION

[00026]   A high Q micro-electromechanical (MEMS) resonator is described which operates as a displacement controlled varactor. When placed in series with a DC voltage source and a circuit to be driven (referred to as the "load"), the varactor becomes a voltage divider which presents a time varying voltage signal to the load. The voltage level rises and falls as energy is transferred back and forth between the mechanical (kinetic) and electrostatic (potential) domains in the resonator system. The resonator can efficiently generate custom-shaped waveforms when biased at or near the natural resonant frequency of the resonator, including resonant energy-recovering AC voltage waveforms. Available AC waveforms include substantially trapezoidal waveforms or triangular waveforms.

[00027]   As used herein, the phrase "substantially trapezoidal" or a "quasi-trapezoidal waveform" refers to a waveform with nearly flat wave peaks and troughs and a gradual transition. Such waveforms can be characterized by (a) a small value (such as 0.01) of the fractional voltage variation $v_V = \Delta V_{var}/\Delta V_{max}$, where ΔV_{var} is the difference between the maximum and minimum voltage over the breadth of the wave peak (or trough), and ΔV_{max} is the difference between the maximum and minimum voltages for the entire waveform, and (b) a small value (such as 0.01) of the maximum relative transition slope $s_{max} = (dV/dt)_{max}$ / $(\Delta V_{max}/\Delta t_{tr})$, where V is the instantaneous voltage, t is real time, and Δt_{tr} is the transition (ramp) time, which is ¼ of the clock period or $\Delta t_{tr} = 1/4f$ in the case of the adiabatic logic family referred to as "2LAL" which described in detail later in this description. Substantially trapezoidal waveforms are ideally suited for driving adiabatic circuits. Other applications such as baseband or ultra-wideband (pulse-based) signaling schemes for RF communications may also benefit from the simplified generation of custom-shaped waveforms provided by the invention.

[00028]   The AC waveform shape can be tailored to nearly any desired shape, by adjusting the

MEMS resonator feature geometry to realize a specific capacitance-versus-displacement

response curve. The vertical profiles of the comb fingers in the alternative embodiments shown

in FIGs. 3(a)-(e) can be easily adjusted to any desired shape, which will have a direct and readily

calculable impact on the capacitance-position response curve and the shape of the generated

output voltage waveform. The inverse problem (to calculate the vertical profile that will produce

a desired given wave shape) can be straightforwardly approximated by differentiating the desired

response curve.

[00029]   MEMS resonators according to the invention can be formed using CMOS-MEMS

processes and can provide quality factors (Q) of 1,000 or more, at frequencies up into the

microwave (GHz) range. Lower-frequency (1-100 MHz range) high Q resonators can also be

provided by the invention for ultra-low-power, low-frequency applications, for which adiabatic

circuits are particularly well suited. The invention can thus replace low Q conventional LC

based electronic oscillators and provide improved circuit performance for a variety of circuit

types.

[00030]   A MEMS resonator according to the invention includes an integrated microstructure

comprising an actuator microstructure and sensor microstructure, each microstructure having a

moving electrically conductive portion and a fixed electrically conductive portion. The shape of

the features comprising either or both the moving portion and the fixed portion of the sense

microstructure are non-uniform, as opposed to conventional MEMS resonators which use

uniformly shaped rectangular electrode fingers. One way to obtain a flat-topped wave shape is to

arrange that the moving portion of the sense microstructure (or at least, the part of it that is

separated by a small gap from the stationary portion) completely overlaps the stationary portion

of the sense microstructure during a significant portion (e.g. at least 25%) of the cycle period.

The non-uniform feature shape provided by the sensor microstructure results in a nonlinear

capacitance-versus-position response curve as the moving portion of the sense microstructure is

moved relative to its fixed portion, and thus to a non-sinusoidal output waveform in the presence

of sinusoidal motion of the movable portion. Applied to adiabatic circuits, the non-sinusoidal

waveform is preferably a substantially trapezoidal waveform which can be obtained by

appropriate resonator geometries determinable using available simulation tools (see Examples

section).

[00031] An exemplary MEMS resonator 200 is shown in Figure 2(a) having applied bias and

excitation voltages applied and driving a load (C_l). Resonator 200 includes actuation

microstructure comprising capacitive actuator portions 211 and 212 and sensing microstructure

comprising capacitive sensors S1, S2, S3 and S4. The number of actuator portions and sensing

portions can be varied from the numbers shown for resonator 200 depending on the desired

application.

[00032] Resonator 200 has quadrilateral symmetry. This layout symmetry is generally

preferred as it can lead to more predictable dynamical behavior of the resonator.

[00033] The shape of the movable and fixed features comprising capacitive sensors S1, S2,

S3 and S4 shown in FIGs. 2(a) –(c) are non-uniform as they have bulbous "capped" ends.

Movable portions of the actuator and sense microstructure are physically anchored to the

substrate through a spring beam 225. Spring beam 225 is free to vibrate in the plane of the chip

bounded by maximum amplitude position generally symmetric about its rest position. As spring

beam 225 moves back and forth in response to an oscillatory excitation signal applied to the

actuator 211 and 212, the capacitance of sensors S1-S4 changes as a result. Figure 2(c) shows the

position of one of the sensors (S1–S4) when the resonator beam 225 is at its maximum displacement position.

[00034]   The circuit driven by resonator 200 denoted by C_l is shown connected to the fixed electrode of S4 (denoted Vo), although S1-S4 are generally all connected to C_l . Through various combinations of S1- S4, frequency and/or amplitude doubling can be obtained as described below. By connecting S1-S4 all directly to the load, an effective doubling of frequency is provided. Each time the moving structure of resonator 200 makes 1 complete cycle, this leads to an overlap of the sense fingers first on one side (S1, S2) , then on the other (S3, S4). Accordingly, the output signal provided by resonator 200 makes 2 cycles in the time for one displacement cycle.

[00035]   The actuator, sense and load capacitances of resonator 200 are denoted as C_a, C_s, C_l in the equivalent circuit shown in FIG. 2(b). C_a and C_s are shown as being variable capacitors. Changes to C_a and C_s result in changes to the voltage across C_l (the device being driven).

[00036]   During normal operation, a DC bias voltage V_b is applied to the movable comb fingers of both actuation and sensing microstructures, while an optional DC voltage plus an AC voltage signal ($V_c + v_{ac}$) is applied to the stationary comb fingers of the actuation structure 211 and 212.

[00037]   The movement of spring beam 225 is stimulated by a sinusoidal (or more generally, any arbitrary-shaped periodic AC) excitation driving signal v_{ac} presented at the stationary actuator electrodes, with a frequency at or near the structure's resonant frequency. The natural resonant frequency of the structure is given by $\omega_r = (k/m)^{1/2}$, where k and m are respectively the spring constant and mass of the resonator. The drive frequency is preferably within the 3-dB bandwidth, i.e., $|\omega\text{-}\omega_r|<\omega_r/Q$, where Q is the quality factor of the resonator and is assumed to be

much greater than 1. The resultant AC electrostatic force resonantly pumps up the amplitude of

the oscillations of the movable portion of resonator 200. The mode of motion of resonator 200 is

that the central arm of spring beam 225 flexes back and forth. The moving portions of actuator

and sensor microstructures comprising features on either side of spring beam 225 are anchored to

its center point and thus also move in the same direction.

[00038]   There are output signals available from each of the four sensing elements S1-S4. S1

and S2 are in phase, as is S3 and S4. S1 and S2 are 180 degrees out of phase with S3 and S4.

Thus, S1 and S2, and S3 and S4 can be utilized differentially to double the amplitudes of the

output signals. Alternatively, S1 and S3, and S2 and S4 can be respectively tied together

electrically to double the frequencies of the output signals as noted above. As a further

alternative, all four sensing elements (S1-S4) can be tied together (i.e., electrically connect all

four fixed electrodes of S1-S4) to double both the frequency and the amplitude of the output

signal provided by resonator 200.

[00039]   As noted above, electrode features comprising the sensing microstructure (S1-S4) are

non-uniform in shape having bulbous capped ends as opposed to conventional designs where the

electrodes features are rectangular. Other non-uniform shapes may be utilized, such as triangular,

trapezoidal or curved. The desired non-linearity of the resonator output is obtained by tailoring

the electrode shape of the MEMS capacitors. Since a resonator begins sinusoidal mechanical

vibrations whenever it reaches resonances, custom waveforms are generated with sinusoidal

mechanical vibration for resonators according to the invention operating at high Q.

[00040]   Regarding the comb fingers with caps shown in FIG. 2(c), it is noted that the sides of

the caps (which carry most of the electrical field) are completely overlapping the walls of the

surrounding finger edges at the maximum amplitude position, and are separated from them by a

relatively narrow gap (denoted d_s in FIG. 2(c)). The small gap provides a large sensing capacitance. The non-uniform shape of features of sensing microstructure are such that the capacitance of S1-S4 changes in a non-linear fashion with respect to the displacement of spring beam 225. This unconventional non-uniform comb finger geometry thus creates a non-sinusoidal waveform when the spring beam 225 oscillates sinusoidally.

[00041]   In contrast, in a conventional MEMS resonator, it is desired to minimize the non-linearity and obtain an ideal sine wave. In practice, a roughly sinusoidal waveform is generated when the resonator beam oscillates sinusoidally. The conventional desired sinusoidal wave shape is produced by partially overlapping, straight linear plates or fingers wherein the capacitance changes linearly with the displacement.

[00042]   The resonator 200 can be made of various materials including polysilicon or single-crystal silicon depending on the available microfabrication technology. In a preferred embodiment, electrodes comprising resonator 200 are formed from single crystal silicon or other pure-crystalline materials. In the future, higher-stiffness materials, such as diamond, may become preferred once their associated processing technologies become more mature.

[00043]   MEMS technology is preferably used to form resonator 200 because of the small size and the high Q factor and high frequency (up into the GHz range) possible using MEMS. Several fabrication processes already exist that can produce MEMS elements integrated with CMOS electronics on the same chip. The sinusoidal waveform that would normally be produced by a DC voltage applied to an oscillating MEMS structure can be remapped into a trapezoidal format by tailoring the shape-profile of the structures (e.g., comb fingers) that are used for electromechanical transduction. High Q can be achieved by reducing gas and structural damping using vacuum packaging and low-loss materials such as single-crystal silicon.

[00044]   As noted above, MEMS Resonator 200 is preferably single-crystal silicon based and CMOS-compatible. CMOS compatibility enables the formation of resonator 200 on-chip with various analog and/or digital electronic circuits.

[00045]   The electrostatic force generated by the actuation features comprising comb fingers is given by:

$$
\begin{aligned}
F_e &= \frac{1}{2}\frac{\partial C_a}{\partial x}\left(V_p + V_{ac}\cos\omega t\right)^2 \\
&= \frac{1}{2}\frac{\partial C_a}{\partial x}\left(V_p^2 + \frac{V_{ac}^2}{2} + 2V_p V_{ac}\cos\omega t + \frac{V_{ac}^2}{2}\cos 2\omega t\right),
\end{aligned} \tag{6}
$$

where $V_p = V_c - V_b$. In order to suppress the second harmonic term, V_p is preferably set much greater than V_{ac}. When operating at its resonant frequency, the vibration amplitude of the fundamental frequency term will be multiplied by a factor of Q and will be the dominant term for the force. The maximum applied voltage which can be used is limited by the oxide breakdown and the air breakdown voltage. Since the resonator 200 shown in FIGs. 2(a) and (c) has a small air gap (~ 0.1 μm; denoted by d_s), air breakdown will generally be the dominant voltage limiter. The air breakdown voltage is approximately 110 V per one μm air gap. Accordingly, the maximum applied voltage is about 10V. Simulations performed have indicated that sufficient displacement can be achieved at $V_p = 10V$. The output voltage V_o can be much smaller than 10V, depending on the load capacitance, and will be tuned to the transistor operating voltage. Due to the high impedance output node, a buffer or operational amplifier can be used to drive the bonding pad for testing purposes.

[00046]   Major figures of merit (quantities to maximize) for resonators according to the invention include:

1. **Effective quality factor** for transitions $Q_{eff} = E_{tr}/E_{diss}$, where E_{tr} is the energy transferred to or from the load on each transition, and E_{diss} is the energy dissipated in the resonator per clock cycle.

2. **Area-efficiency** $\alpha_E = A/E_{tr}$, where A is the resonator area and E_{tr} is the energy transferred. This determines the ratio between the area consumed by the resonator and that consumed by the logic, which contributes to the cost overhead of the adiabatic solution.

Major figures of demerit (quantities to minimize) for the resonator design include:

1. **Maximum transition slope** $s_{max} = (dC/dt)_{max} /(\Delta C_{max}/\Delta t_{tr})$, where C is the instantaneous sense-structure capacitance, t is real time, ΔC_{max} is the total capacitance swing needed to obtain the desired voltage variation, and $\Delta t_{tr} = 1/4f$ is the transition time, ¼ of the clock period in the case of two-level adiabatic logic referred to as 2LAL described below. Ideally the entire capacitance swing should occur at a constant rate, in which case $s_{max}=1$, but a non-ideal waveform might have a steeper slope than this in some places. The s_{max} value permits derivation of an upper bound on the total energy dissipation of the logic transition, as a multiple of that for the ideal ($s_{max} = 1$) case.

2. **Fractional capacitance variation** $v_C = \Delta C_{var}/\Delta C_{max}$, where ΔC_{var} is the maximum range of sense-structure capacitance during the ¼ of a cycle during which the capacitance (and output voltage) is supposed to remain constant. This can be used to provide an upper bound on the maximum voltage mismatch ΔV that may occur whenever two circuit nodes are connected that are nominally supposed to be at equal logic levels; this mismatch leads to a $\frac{1}{2}C(\Delta V)^2$ dissipation that would not occur in the ideal case.

[00047]   Finally, the resonant frequency f of the resonator structure should not itself

necessarily be minimized or maximized, but rather should be chosen so as to maximize the

overall power-performance (or cost-performance) of the overall design, that is, the resonator

together with the logic.

[00048]   Figures 3(a) –(e) show exemplary alternative non-uniform comb finger shapes

surrounded by a pair of fixed plates, according to other embodiments of the invention. In each of

these alternate embodiments, the entire moving plate is overlapping the fixed plate structure,

except for a short arm which extends up (or down) vertically to an overhead mechanical support.

These embodiments increase the magnitude of the capacitance variation while reducing the

magnitude of departures from the trapezoidal wave shape desired for adiabatic circuits. In

addition, these designs maximize the vertical (z) thickness for maximum overlap capacitance per

planar area, and minimize the gap size for maximum overlap capacitance per-area.

[00049]   The shape of the capacitance-versus-position response curve, and the output

waveform, can be fully tailored in these designs by adjusting the height profile of the fixed

and/or moving plates. Optimized shape tailoring requires solving a complex inverse problem.

One way to approximately solve this problem involves differentiating the desired capacitance-

position response curve to obtain the thickness (z) profile of a moving plate that will produce

approximately the desired response curve (neglecting fringing capacitances) as it crosses the

edge of a larger stationary plate. An initial design obtained in this fashion can then be fine-tuned

by hand or automatically with the assistance of electrostatic solvers to yield a near-exact match

to the desired shape.

[00050]   Based on the design and analysis work already performed, MEMS resonators

according to the invention will provide an effective Q factor as high as 100 or more, using an

area not much greater than that of the logic circuit being driven. The resonator Q can be increased further by systematically identifying and eliminating the major sources of power dissipation. Leakage losses in the logic circuitry can be reduced exponentially by slight (logarithmic) up-scaling of the operating voltage and device size. In the long run, the cost of these small increases are more than outweighed by the power-performance advantages of the adiabatic approach, and by improvements in manufacturing efficiency. Circuit size will not be a limiting concern in the near future with the introduction of 3-D integration techniques, made feasible by the ultra-low power dissipation of the adiabatic design.

[00051]   In this application, the adiabatic logic design style 2LAL described above that was developed by one of the Inventors is utilized herein to aid in describing the invention. MEMS resonators according to the invention are well suited for resonantly generating (with high Q, such as >100) the 4-tick trapezoidal waveforms needed to drive the 2LAL circuits. Although well suited for this purpose, the invention is in no way limited to application to adiabatic circuits.

[00052]   As per its name, 2LAL uses two distinct voltage levels (high and low), analogous to e conventional CMOS, but unlike some earlier adiabatic logic styles such as SCRL (Split-Level Charge Recovery Logic). Nevertheless, 2LAL has some desirable properties of SCRL, such as being fully adiabatic and permitting pipelined sequential circuits. Further, 2LAL fixes a bug causing non-adiabatic dissipation that was present in the original version of SCRL. 2LAL also has some particularly desirable other properties including:

1. **Short cycle time**: only 4 adiabatic transition times (4 ticks) per complete clock period.

2. **Low latency**: only 1 tick of latency per logic level / pipeline stage.

3. **Low number of supply rails**: only 4 distinct driving signals need be supplied.

[00053]   The first of these properties implies a low initiation interval (thus high throughput)

for pipelines built from 2LAL gates. Also, transitions take place over an entire ¼ of the clock

cycle, which is the maximum possible in fully-adiabatic logic. This minimizes the energy

dissipation for transitions occurring at a given clock frequency. It also minimizes the slope of

the transitions, which makes it easier to obtain the desired slope in the resonant power supply

(see next section), and minimizes the duty cycle (active high time / cycle time), which makes it

easier for the power supply to keep the high/low signal levels constant. In essence, a cycle time

of 4 ticks means a trapezoidal signal that is as close as possible in shape to a sine wave and thus

is easiest for a resonator to generate with high Q (since the energy in the higher-order harmonics

is lower).

[00054]   The second property, of only 1 transition time or "tick" of latency per logic level

guarantees the minimum possible time for information to propagate down a logic pipeline, given

the transition time, and thus minimizes stalling for data-dependent operations.

[00055]   The third property, low number of supply rails, minimizes the area required for im-

plementing the resonators, since as few as possible of them are needed. At least 4 supply signals

are needed for fully-adiabatic logic. Figure 3 shows the rails needed for 2LAL. The basic

elements of 2LAL logic circuits are described in Figure 4.

[00056]   Current designs are performed using Cadence for these and other basic 2LAL cells,

as well as higher-level blocks such as single-bit and multi-bit adders and multipliers.

Development of fully-adiabatic DRAM and SRAM cells is also ongoing. Using the invention, a

complete suite of practical fully-adiabatic building blocks can be built, suitable for constructing

microprocessors, DSPs, and ASICs. A more extensive schematic notation, as well as a VHDL-

like textual hardware description language for adiabatic circuits, and related design tools

specialized for adiabatic design, including circuit synthesis, simulation, and validation tools are also expected to be completed based on principles herein. These would facilitate the design of fully-adiabatic circuits, which is presently somewhat cumbersome when constrained to using traditional languages, design tools, and notations.

[00057]   The invention is expected to have a wide range of applications. Products obtainable from the invention include ultra-low-power (microwatt scale) digital processing components (microprocessors, DSPs, FPGAs, ASICs) for embedded systems based on currently available CMOS technologies. It is expected that extremely power-efficient high-performance processors for tightly-coupled parallel applications (e.g. typical supercomputer applications) in which energy dissipation is a major limiting factor on performance will begin to utilize the invention. In addition, high-performance, energy-efficient computers using nanometer-scale switching elements operating near the limits of physical information encoding efficiency, regardless of whether these logic elements are electronic or use other physical domains for information processing (such as electromechanical, mechanical, optical, optoelectronic, spintronic, chemical, or fluidic), as long as adiabatic transitions within the given domain can be driven by the trapezoidal voltage signal generated by these resonators can also benefit from the invention. Higher-level products requiring any of the above components, such as desktop/laptop/server computers, supercomputers, PDAs, wireless communication devices, smart tags, autonomous wireless sensors, implanted medical devices, and nano-robots can also benefit from the invention.

<div align="center">Examples</div>

[00058]   The present invention is further illustrated by the following specific examples, which should not be construed as limiting the scope or content of the invention in any way.

[00059]   A finite-element MEMS simulator CoventorWare® (Coventor, Inc., Cary, NC) was

used to design the non-uniformly shaped sensing comb fingers to generate the desired output

waveforms. One exemplary waveform obtained from the simulation is shown in FIG. 6. The flat

top of the trapezoidal signal is realized by custom tuning the shape of the sense comb fingers,

such as the capped fingers shown in FIG. 2(a) and (c). The nearly flat bottom of the waveform is

due to the very small change of the fringing capacitance when the moving fingers are far from

the stationary fingers.

[00060]   As shown in FIG. 2(a), when resonator 200 is at rest, the moving and stationary

sensing comb fingers are separated by 3 μm. When the resonator moves to the maximum

amplitude position, as shown in Figure 2(c), the minimum gap d_s between the (moving and

stationary) sense comb fingers is as small as 0.1 μm. Gaps less than 0.1 μm are also achievable,

but the maximum applied voltage will then need to be decreased due to air breakdown. Some

design parameters are shown in Table 1 below. A 20 fF sense capacitance variation was

achieved.

Table 1. Some key parameters of a prototype resonator at 0.5 MHz resonant frequency.

Thickness:	2 μm	Bias voltage V_b:	10 V
Min. gap size:	0.1 μm	DC drive voltage $|V_c-V_b|$:	10 V
Min. feature size:	0.5 μm	AC drive voltage v_{ac}:	0.2 V
# of actuation fingers N_a:	20	Area A:	107 μm ×36 μm
# of sensing fingers N_s:	106	Capacitance variation:	20 fF
Quality factor Q:	5000 (est.)	Effective quality factor Q_{eff}:	46
Vibration amplitude X:	4 μm	Area efficiency α_E	3.23×10^{-4} J/m^2

[00061]   The sensing capacitance variation is only ~0.2 fF per comb finger. However, it should be feasible to increase the structure thickness by a factor of 20 using an available Deep Reactive Ion Etching (DRIE) process which can yield a figure closer to 4 fF per comb finger. Using a bias voltage of 10 V and 10 comb fingers, this means each comb finger could drive a load equivalent to about 40 minimum sized devices of about 1 fF load capacitance each, through a voltage swing of ~1V. The area needed for this many devices is close to the area occupied by the comb finger.

[00062]   A prototype design with somewhat lower resonant frequency using the Taiwan Semiconductor Manufacturing Company (TSMC) 0.35 μm CMOS process was taped out. The 3D model of the submitted design is shown in FIG. 7. This is a resonator prototype with much larger size which can generate the trapezoidal waveform at much lower frequency (around 100 kHz). The total area is 300 μm by 160 μm. In this design, the effective quality factor and area efficiency are not optimized. The parameters for this resonator are listed in Table 2. The resonant frequency can be scaled up with a smaller resonator.

Table 2. Some key parameters of the prototype 100 kHz resonator shown in FIG. 7.

Thickness:	30 μm	Bias voltage V_b:	10 V
Min. gap size:	0.5 μm	DC drive voltage $|V_c - V_b|$:	50 V
Min. feature size:	2.5 μm	AC drive voltage v_{ac}:	2V
# of actuation fingers N_a:	48	Area A:	300 μm × 160 μm
# of sensing fingers N_s:	24	Capacitance variation:	30 fF
Quality factor Q:	5000 (est.)	Effec. Qual. factor Q_{eff}:	0.16
Vibration amplitude X:	16 μm	Area eff. α_E	1.1×10^{-4} J/m^2

To optimize the resonator design requires a joint system-level optimization in concert with the logic, in order to select the optimal operating frequency, voltages, and resonator area so as to maximize the overall gain in cost-performance from the adiabatic design. A complete analysis that does this has not yet been done, since alternative resonator geometries are still being explored. However, some aspects of the resonator design have already been optimized. From the resonator point of view, given the limitation of air breakdown voltage, the optimization of Q_{eff} and α_{E} is done by maximizing the sense capacitance variation and minimizing the vibration amplitude and the resonator area. New regions of the design space need to be explored to further improve these parameters.

[00063]   Simulations based on BSIM3 device models were performed to calculate the maximum operating frequencies for logic in the TSMC 0.18 μm CMOS technology presently used for designing the 2LAL test circuits. Preliminary results show that, at an example ultra-low power level of 7 pW per logic gate, standard CMOS can run at a maximum frequency of only 80 kHz, by operating in a subthreshold regime of $V_{dd} = 180$ mV, while adiabatic CMOS can run at up to 3.9 MHz, at a much higher voltage of 1.7 V, while still satisfying the power constraint. The adiabatic performance boost is thus about 50× and the cost-efficiency boost is about ~12x in the application scenario used (with 4× overhead).

[00064]   Although the peak frequency of ~4 MHz in this scenario is a little higher than achieved in the present resonator prototypes, further design refinements in a newer MEMS process should be able to easily move the invention well into the MHz frequency range. Once this is done, based on the preliminary analyses performed, it is expected to be able to empirically demonstrate roughly an order-of-magnitude reduction in energy dissipation in our MEMS/2LAL design compared with standard CMOS, when optimized using the design methodology described

herein. As MEMS technology pushes down towards the nanoscale, further refinements of these techniques are expected to lead to significant boosts in both performance and cost-performance for particularly power-limited applications in the near-term, and in the long term for most high-performance computations.

[00065] As noted above, in certain applications, adiabatics can provide improved results as compared to conventional approaches. With conventional voltage scaling, severe limitations are encountered due to the substantially increased effective resistance (and low on/off ratio) suffered by devices operated in the low-voltage regime. The high effective resistance constrains devices to be operated so slowly that their low on/off ratio severely limits the energy savings that can be achieved, due to the relatively high off-state leakage current, and the substantial resulting standby power consumption. In contrast, the adiabatic approach permits operating energy-efficiently at much higher voltages, at which the effective on-resistance remains small and the on/off ratio remains high, so that leakage is much less of a factor. Moreover, an adiabatic device does not have to be slowed down by as large a factor as a voltage-scaled device in order to achieve a given reduction in power dissipation, due to the quadratic (rather than linear) scaling of power with frequency. The end result is that at a given low level of power dissipation, the adiabatic approach can ultimately offer higher performance than any competing approach in the same process technology.

[00066] Figure 8 shows simulation results based on an optimization analysis using a standard device model for the TSMC 0.18μm process technology confirming the performance advantage in maximum frequency vs. power dissipation provided by adiabatic circuits as compared to a conventional voltage scaled circuit. The upper line in FIG. 8 shows the adiabatic circuit while the lower line shows the conventional voltage scaled circuit. At low power levels, the

conventional voltage-scaling approach suffers from reduced drive current (increased effective channel resistance) at low supply levels, which limits the maximum operating frequency to a level that is at most roughly proportional to power. In contrast, the adiabatically switched device can continue to be operated at the recommended voltage of the technology (1.8 V), while performance falls off more slowly, roughly with only the square root of the power drop. Near the left of the FIG. 8, it can be seen that by the time an ultra-low-power level of 6.3×10^{-12} W (roughly 10 pW) per device is reached, near the lower limit set by leakage power, the adiabatic device is running at ~50× the conventional one's frequency (12.7 MHz vs. 260 kHz) in this particular Example.

[00067]   This invention has been described herein in considerable detail to provide those skilled in the art with information relevant to apply the novel principles and to construct and use such specialized components as are required. However, it is to be understood that the invention can be carried out by different equipment, materials and devices, and that various modifications, both as to the equipment and operating procedures, can be accomplished without departing from the scope of the invention itself.

CLAIMS

We claim:

1.   A MEMS waveform generator, comprising:

a electrostatic actuator microstructure, said actuator having a movable portion including a plurality of movable electrically conductive features and a fixed portion having a plurality of electrically conductive features, said fixed actuator portion for receiving a time varying input signal and oscillating a position of said movable features in response, and

a capacitive sensor microstructure, said capacitive sensor having a movable portion comprising a plurality of movable electrically conductive features and a fixed portion having a plurality of electrically conductive features, said movable features of said sensor physically coupled to said movable features of said actuator, wherein at least a portion of said sensor features are non-uniformly shaped.

2.   The MEMS generator of claim 1, a spring beam physically couples said movable features of said sensor and said movable features of said actuator to said substrate.

3.   The MEMS generator of claim 1, wherein at least a portion of said features are formed from single-crystal silicon.

4.   The MEMS generator of claim 1, wherein said generator provides substantially multiple frequency component comprising waveforms responsive to a sinusoidal excitation signal applied to said actuator.

5.   The MEMS generator of claim 1, wherein said sensor microstructure comprises a plurality of sensors.

6.   An electronic device, comprising:

the MEMS waveform generator of claim 1, and at least one electronic circuit connected in series with said generator.

7.   The device of claim 6, wherein said generator provides a substantially trapezoidal output signal responsive to a sinusoidal input signal.

8.   The device of claim 6, wherein said electronic circuit comprises an adiabatic circuit.

HIGH-Q MEMS RESONATORS AND ADIABATIC LOGIC CIRCUITS USING THE SAME

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