



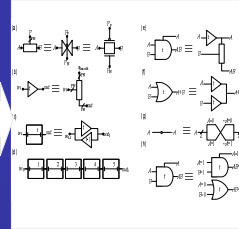
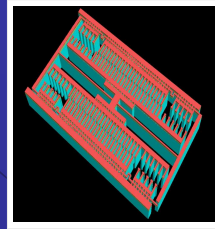
Design & feasibility study for practical adiabatic logic driven by custom high-Q MEMS/NEMS clock/power resonators



Departments of ECE and CISE

Introduction

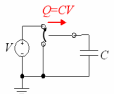
The key barrier that in the past has prevented adiabatic (thermodynamically reversible) logic-circuit design techniques from becoming a practical approach for ultra-low-power digital computing is the lack of energy efficiency in the power supply, due to the low Q factors of AC signal generators that can be built using standard integrated electronics.



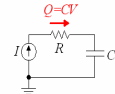
Current Research

In the ADIAMEMS project at the University of Florida, we are designing a custom MEMS resonator for driving fully-adiabatic pipelined logic based on the 2LAL (two-level adiabatic logic) family previously developed at UF. The resonator design is being optimized so as to maximize its effective Q factor and area efficiency, at an operating frequency chosen to maximize the power-performance of the adiabatic logic.

- Conventional charging:
 - Constant voltage source
- Ideal adiabatic charging:
 - Constant current source



$$E_{\text{diss}} = \frac{1}{2} CV^2$$



$$E_{\text{diss}} = I^2 R t = \frac{Q^2 R}{t} = CV^2 \frac{RC}{t}$$

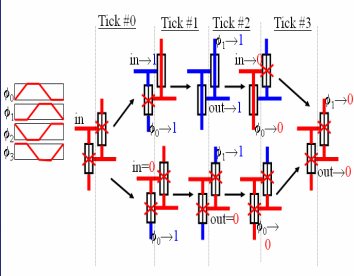
$$\text{Advantage factor } A = \frac{1}{2} CV^2 / (CV^2 RC / t) = t / 2RC$$

ADIABATIC LOGIC DESIGN

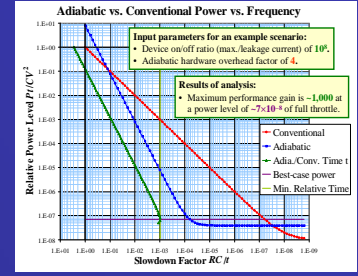
- Avoiding passing current through diodes
- Never turn on a transistor when $V_{DS} \neq 0$
- Never turn off a transistor when $I_{DS} \neq 0$
- "The logic design must be logically reversible"
- Leakage Power should be kept Manageable

- Use a voltage ramp to approximate an ideal current source.
- Switch conditionally, if MOSFET gate voltage $V_g > V + V_T$ during ramp.
- Can discharge the load later using a similar ramp.
 - Through the same, or a different path.

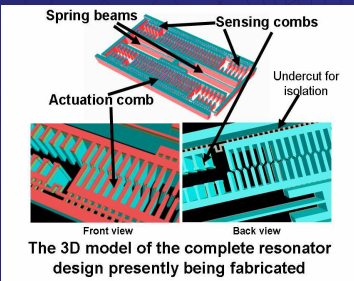
$$t \gg RC \Rightarrow E_{\text{diss}} \rightarrow CV^2 \frac{RC}{t} \quad t \ll RC \Rightarrow E_{\text{diss}} \rightarrow \frac{1}{2} CV^2$$



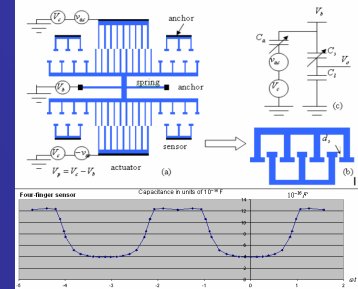
- In tick 0, the input transitions to 1 (at the same time as Φ_0), and the output switch turns on.
- In tick 1, Φ_1 goes high (unconditional bias) taking the output with it. This turns on the reverse switch.
- In tick 2, the input is retracted from its source, turning off the output switch. The output information is latched into place.
- In tick 3 Φ_0 reverts to its low state which does not affect anything inside the circuit but prepares us to be able to turn on the forward switch again in the next cycle. Meanwhile, the next gate in the chain restores the output to the zero level.



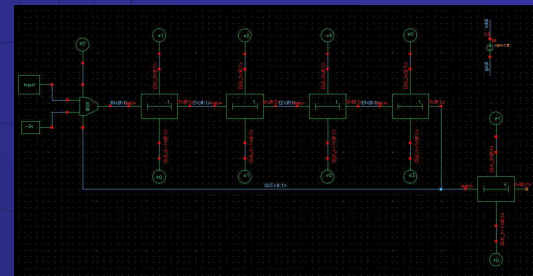
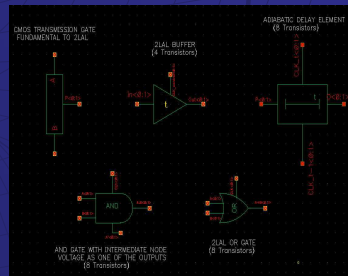
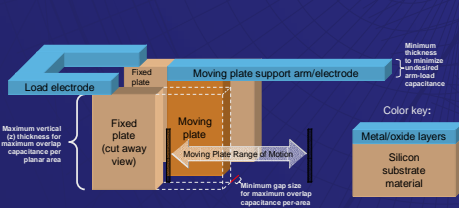
MEMS RESONATOR DESIGN



- Figure (a) The resonator design.
- Figure (b) The sensing structure composed of comb fingers with a wide portion at the end. This unusual comb finger geometry is used to create a non-sinusoidal waveform when the resonator oscillates sinusoidally.
- Figure (c) The sensor position when the resonator beam oscillates to the maximum amplitude position.
- Symbols: V_b =resonator bias, V_c =DC actuator bias, v_{ac} =amplitude of AC actuator bias, C_a, C_s, C_l =actuator/sense/load capacitances.



DESIGN SCHEMATICS



- In the AdiaMEMS project at UF, we are taking the first steps towards demonstrating adiabatic techniques that can actually be commercially practical for ultra-low-power logic.
- A prototype MEMS resonator producing a high quality custom wave shape was successfully designed and sent out for fabrication.
- Simulations on new 2LAL design style indicate that a 50x performance boost might be achieved versus conventional CMOS in ultra-low-power application scenarios in a presently available process technology.

Regarding the future promise of adiabatics, we can declare: "You ain't seen nothin' yet"



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